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DIGITAL READ-OUT FOR VHF/UHF RECEIVER

Real-time Clock for 80C32 Computer

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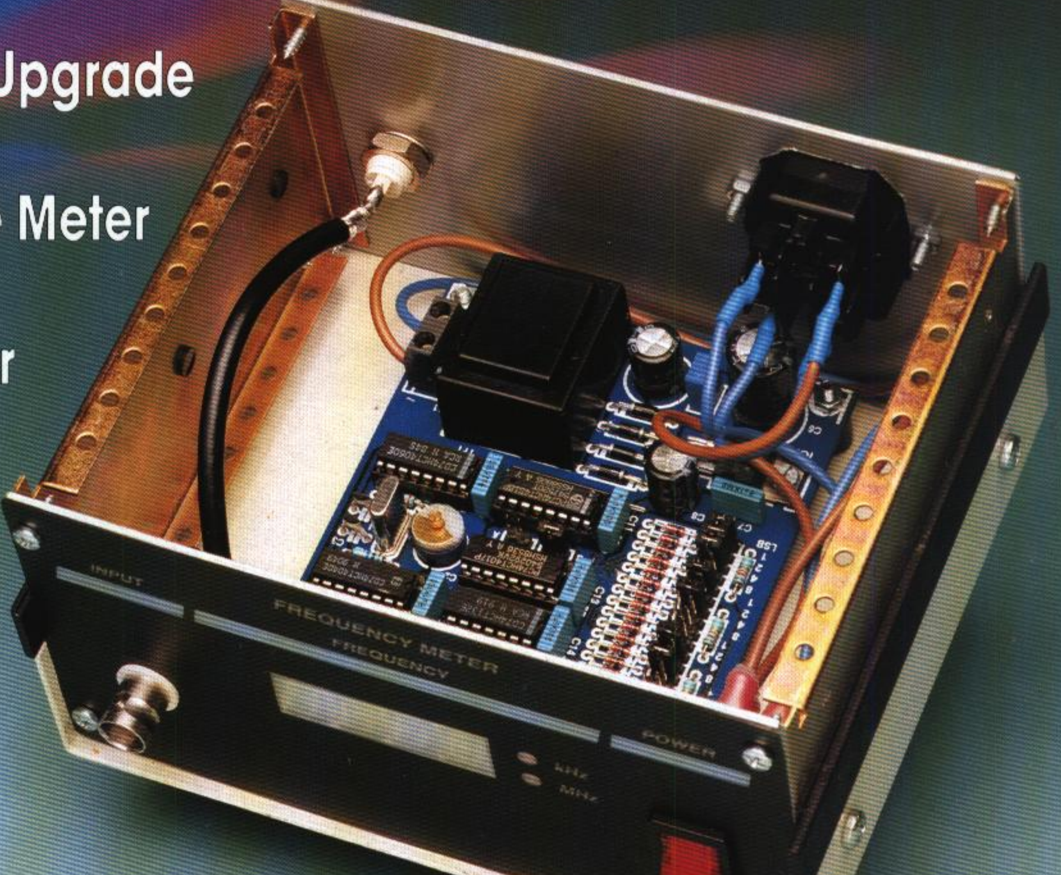
Inexpensive Phase Meter

Spectrum VU Meter

Electricity from the Wind

A CW Compatible T/R Switch



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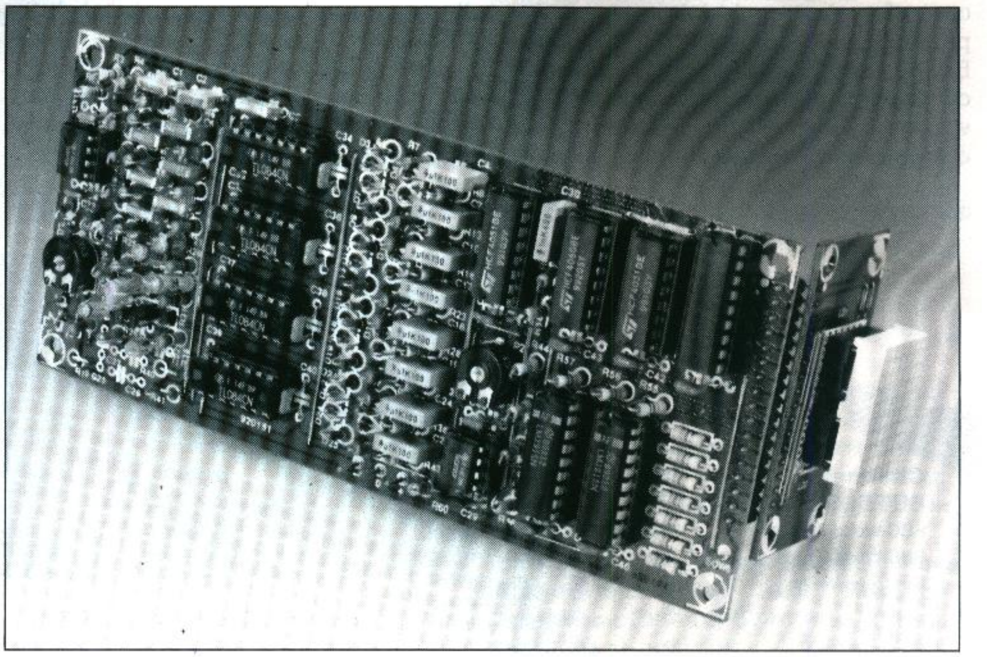
SPECTRUM VU METER

Design by T. Giesberts

Making an audio signal visible on a display is something that appeals to many audio & hi-fi enthusiasts. Most commercial audio equipment is now provided with a display in the form of one or more light bars that move in rhythm with the music. The proposed VU meter offers seven or eight bars that each serve a certain part of the audio spectrum.



A VU meter used to be a moving-coil meter that indicated the drive power of, for instance, a tape recorder in 'Volume Units'. Modern equipment is normally provided with a VU meter consisting of a bar of small LEDs per channel.

The VU meter described is intended primarily for use with an amplifier and does not only show the strength of the incoming or outgoing signal, but also its spectral distribution. The sound spectrum is divided into seven or eight bands, each of whose strengths is shown on a 10-LED bar. All these LEDs do not present a construction problem, because use is made of two 5×7 or 5×8 matrix displays that are mounted one above the other. These displays are available in various sizes, from 18×26 mm to 61×72 mm.

Design considerations

The audio input signal is fed to a variable amplifier and then to seven filters (Fig. 1). The eighth filter shown is for use only with large displays that have eight LED bars. The lowest filter is a low-pass section, the five (or six in case of a large display) following ones are band-pass sections, and the highest is a high-pass section. To obtain a good split of the audio spectrum and yet keep the number of components in the filters to a minimum, the cut-off frequencies and Q factors have been chosen to give –10 dB transfer points of adjacent frequencies. That may seem a lot, but it should be borne in mind that the resolution of the display is 3 dB per step at the top and as much as 9 dB per step at the bottom.

To get an even distribution of the audio range of 20 Hz to 20 kHz, the central frequencies of the band-pass filters have been set to 130 Hz, 340 Hz, 880 Hz, 2.3 kHz, and 6 kHz. With a Q factor of 3, the filters interconnect just about at their –10 dB points.

The cut-off frequency of the low-pass filter is set to 50 Hz and that of the high-pass section to 15 kHz. For small displays, these filters are third-order Butterworth types that fit in well with the band-pass sections, but for large displays their behaviour becomes more of a Chebishev nature.

The filter responses are shown in Fig. 2.

The filter outputs are passed to peak detectors. These are rather more complex than in Fig. 1, but that will be reverted to in the circuit description.

The seven (eight) direct voltages are fed to a multiplexer that passes one of them via buffer-amplifiers to a double comparator-buffer formed by two LED driver ICs. These quasi-series connected ICs enable a range of some 50 dB to be displayed.

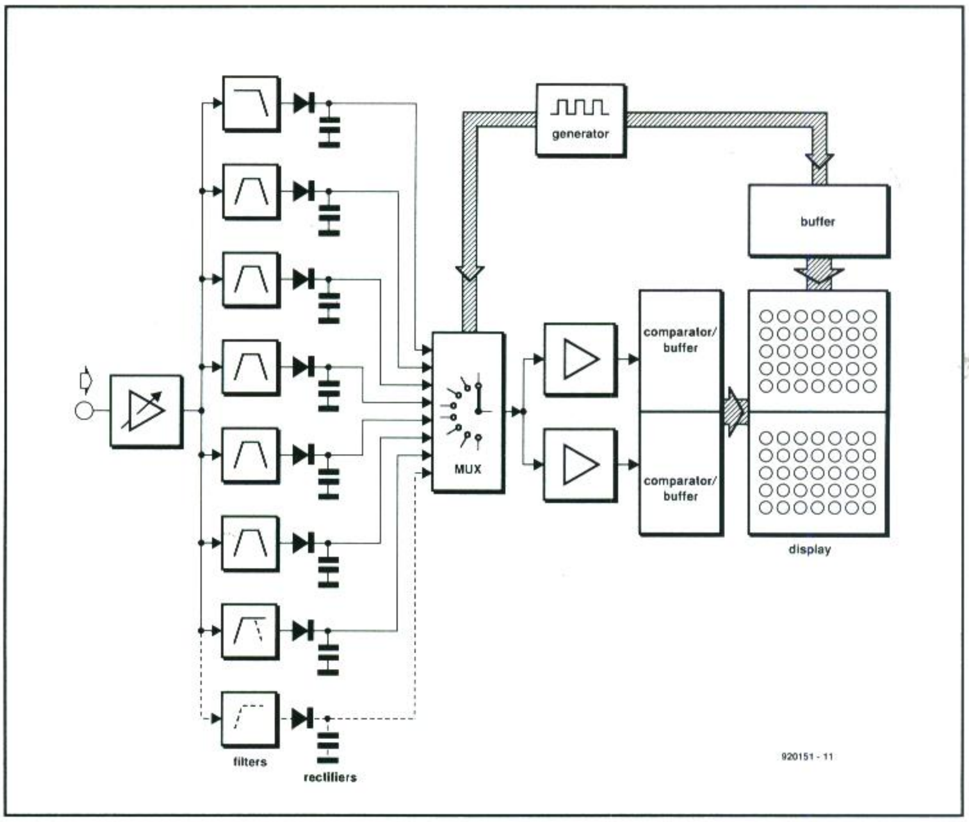


Fig. 1. Block schematic of the VU meter.

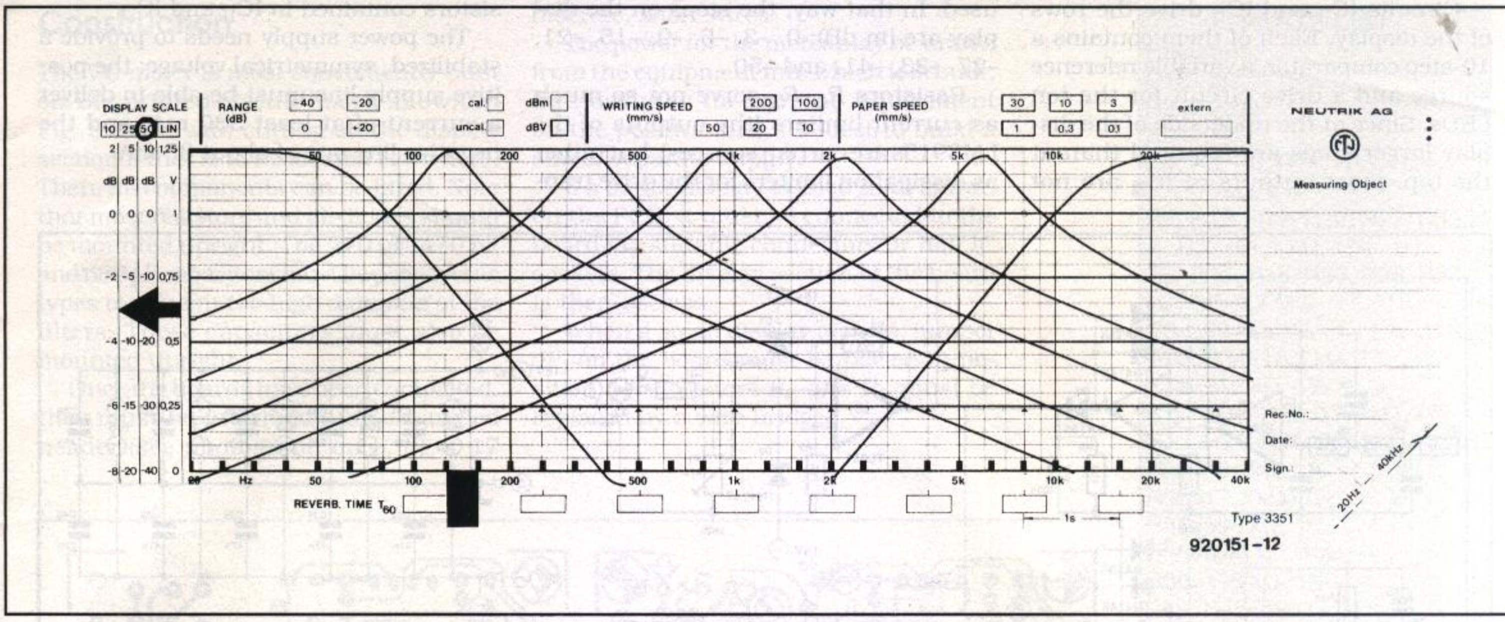


Fig. 2. Response curves of the low-pass, high-pass and band-pass filters when a seven-bar display is used.

A frequency generator provides the clock that switches the multiplexer to each successive direct voltage. At the same time, this signal actuates the LED bar associated with that direct voltage via a number of buffer stages, so that this bar displays only the level monitored at that instant.

The circuit

The audio input is applied to K_1 (see Fig. 4) and from there to IC_1 via P_1, which enables it to be attenuated as required. The amplifier has a gain of about 16 dB. The output of IC_1 is fed to the seven or eight filter sections. The multiple feedback band-pass filters are formed by IC_{2a}, IC_{3d}, IC_{3a}, IC_{4d}, and IC_{4a}. As already mentioned, their Q factor is 3.

The third-order low-pass filter, which has a cut-off frequency of 50 Hz, is based on IC_{2d}.

The third-order high-pass filter, which has a cut-off frequency of 15 kHz, is based on IC_{5d}.

If a 10×8 LED matrix is used, the eighth filter needed is based on IC_{5a}. In that case, the high-pass filter based on IC_{5d} is converted to a band-pass section (whence the duplicated component indications; in the C_{20} position a resistor is then used). Table 1 lists all the component values in case eight filters are used.

The rectifiers are pseudo-active types to ensure proper coverage of the display range of 50 dB. In the prototype, standard passive rectifiers, even Schottky types, gave serious deviations (in some case, a 30 dB signal was attenuated to no less than 12 dB by the rectifier). The design finally chosen consists of a passive rectifier, consisting of a diode (D_5, D_8, D_{11}, D_{14}, D_{17}, D_{20}, D_{23}), a capacitor (C_4, C_7, C_{10}, C_{13}, C_{16}, C_{19}, C_{24}) and a discharge resistor (R_8, R_{13}, R_{18}, R_{23}, R_{28}, R_{33}, and R_{38}), coupled with an active compensating device (IC_{2c}, IC_{2b}, IC_{3c}, IC_{3b}, IC_{4c}, IC_{4b}, and IC_{5c}).

The active devices compensate the forward bias of the associated diodes as well as the discharge of the capacitors through the diodes when these conduct.

Since each of the ICs, connected in a voltage follower configuration, has negative feedback through two anti-parallel diodes, its output will always be larger by the forward bias of one of the diodes (D_3, D_6, D_9, D_{12}, D_{15}, D_{18}, D_{21}) than the input. That bias depends to some extent on the current, which here is determined by the load resistor (R_7, R_{12}, R_{17}, R_{22}, R_{27}, R_{32}, R_{37}). The diodes mentioned above are of a type that is identical to the rectifier. The type of the other diode in the feedback loop is not so important.

When the input is small, the drop across D_3, D_6, and so on, may be increased by reducing the value of R_7, R_{12}, and so on.

Outputs Q3, Q4 and Q5 of oscillator-divider IC_8 switch multiplexer IC_6 at a frequency of about 400 Hz, so that at all times one of the output voltages of the rectifiers is connected to the comparator and drive section, IC_9, IC_{11}, IC_{12}.

The same three Q outputs of IC_8 are also linked to binary-to-decimal converter (BDC) IC_7. This converter ensures (via a number of buffers contained in IC_{10}) that the LED bar associated with the direct voltage output of the multiplexer at that instant is powered.

When all LEDs of a small display with seven bars light, the average current drawn is 263 mA.

The multiplexer is linked to IC_{11} and IC_{12} via two opamps, IC_{9a} and IC_{9b}. The first serves as a buffer for IC_{11}, while the second not only buffers the signal to IC_{12}, but also amplifies it ×32.

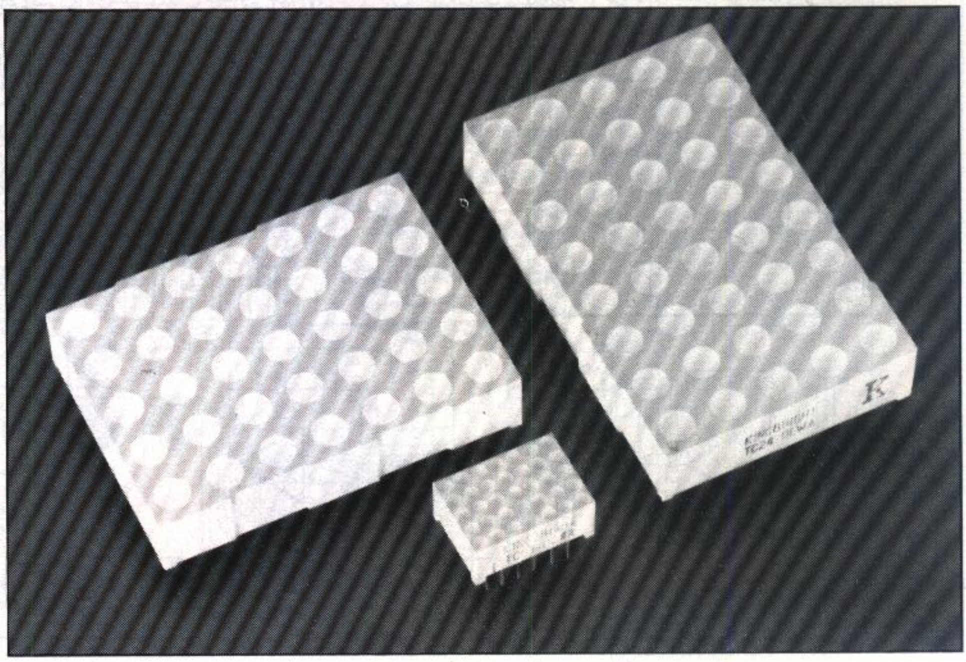


Fig. 3. The displays are available in a variety of sizes.

Circuits IC_{11} and IC_{12} drive the rows of the display. Each of them contains a 10-step comparator, a variable reference source and a drive circuit for the ten LEDs. Since at the underside of the display larger steps are required than at the top, most outputs of IC_{12} are not used. In that way, the steps on the display are (in dB): 0, –3, –6, –9, –15, –21, –27, –33, –41, and –50.

Resistors R_{48}–R_{57} serve not so much as current limiters (the outputs of the LM3915s are current sources), but rather as dissipation limiters for the drive transistors contained in IC_{11} and IC_{12}.

The power supply needs to provide a stabilized, symmetrical voltage; the positive supply line must be able to deliver a current of at least 330 mA, and the negative line one of about 35 mA.

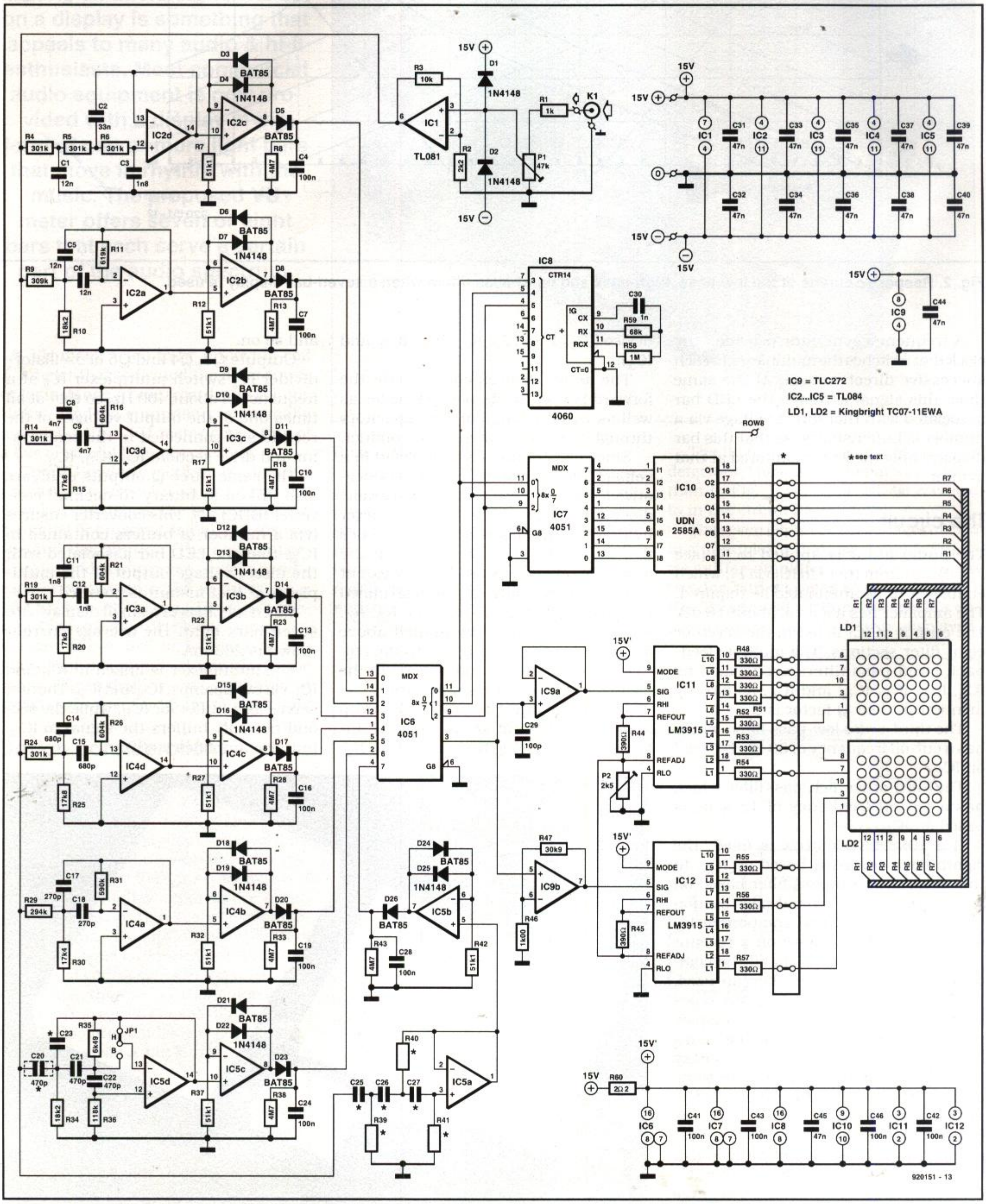


Fig. 4. Circuit diagram of the VU meter.

Construction

The VU meter is most conveniently built on the printed-circuit board shown in Fig. 5. Start with cutting off the display section if that is to be located elsewhere. Then, all components can be fitted. Note that most resistors and all diodes should be mounted upright. The 270 pF, 470 pF and 680 pF capacitors must be polystyrene types to prevent too high damping of the filters. These capacitors must also be mounted upright.

Once the boards have been completed, they must be interlinked by an angled header (see photograph on p. 8) or 17 discrete, short wires.

The power for the meter may be drawn from the equipment into which it is built, but, owing to the current requirement on the positive line, it is best to build a small, separate supply.

If a larger display is used than shown on the PCB, it must be connected to the board via suitable connectors or half IC sockets. The display section of the board is then useless.

When a small display is used, jumper JP$_1$ on the board must be placed in position 'H'. Resistors R_{41} and R_{43} must be replaced by a wire bridge.

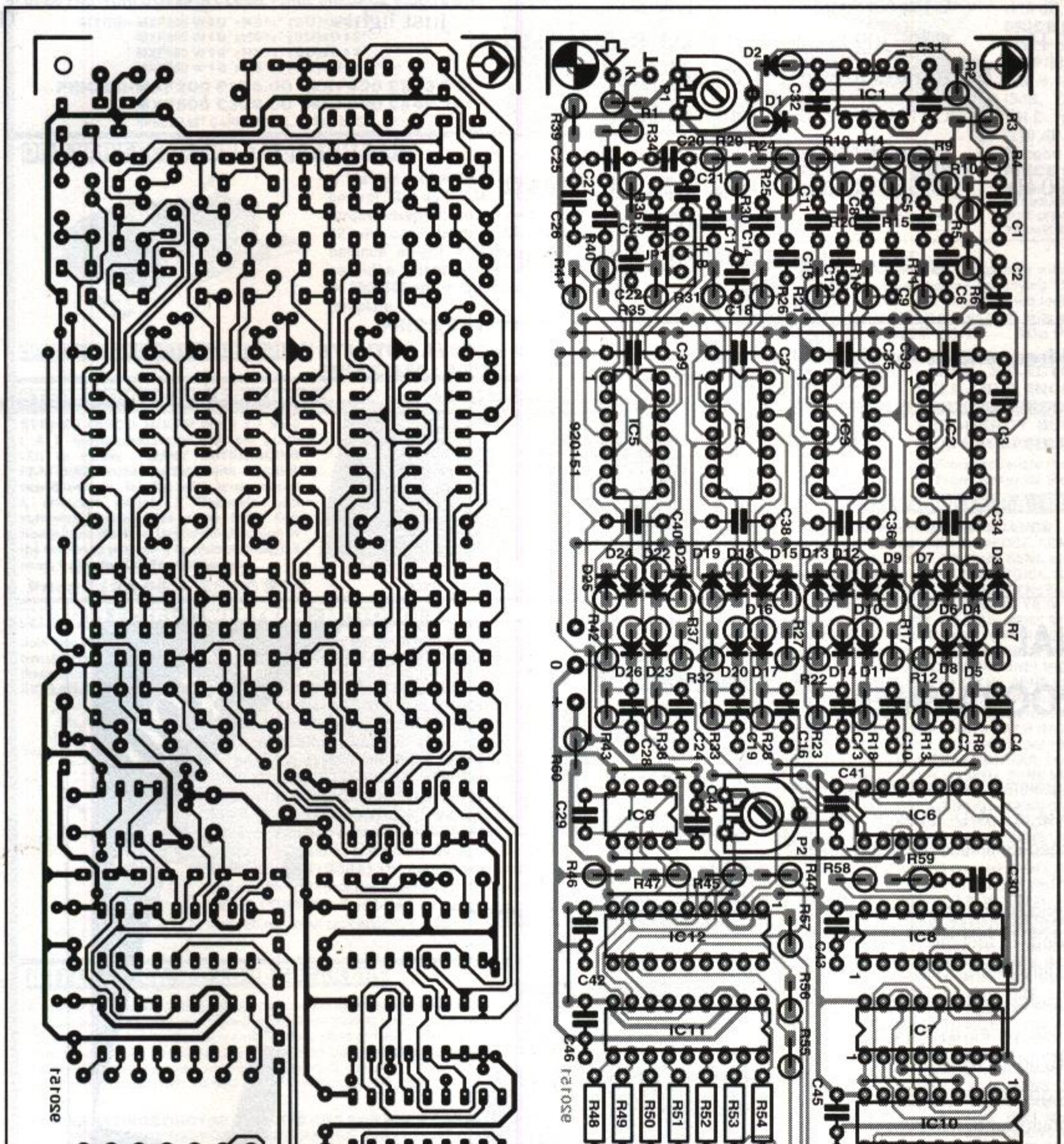


Fig. 4. The printed-circuit board for the VU meter.

PARTS LIST

Resistors:
R1=1 kΩ
R2=2.2 kΩ
R3=10 kΩ
R4, R5, R6, R14, R19, R24= 301 kΩ, 1%
R7, R12, R17, R22, R27, R32, R37=51.1 kΩ, 1%
R8, R13, R18, R23, R28, R33, R38=4.7 MΩ
R9=309 kΩ, 1%
R10, R34=18.2 kΩ, 1%
R11=619 kΩ, 1%
R15, R20, R25=17.8 kΩ, 1%
R16, R21, R26=604 kΩ, 1%
R29=294 kΩ, 1%
R30=17.4 kΩ, 1%
R31=590 kΩ, 1%
R35=6.49 kΩ, 1%
R36=118 kΩ. 1%
R44, R45=390 Ω
R46=1.0 kΩ, 1%
R47=30.9 kΩ, 1%
R48–R57=330 Ω
R58=1 MΩ
R59=68 kΩ
R60=2.2 Ω
P1=47 kΩ preset
P2=2.5 kΩ preset

Capacitors:
C1, C5, C6=12 nF
C2=33 nF
C3, C11, C12=1.8 nF
C4, C7, C10, C13, C16, C19, C24=100 nF
C8, C9=4.7 nF
C14, C15=680 pF*
C17, C18=270 pF*
C20, C21, C22=470 pF*
C29=100 pF
C30=1 nF
C31–C40, C44=47 nF, ceramic
C41, C42, C43, C45, C46= 100 nF, ceramic
*polystyrene, axial

Semiconductors:
D1, D2, D4, D7, D10, D13, D16, D19, D22=1N4148
D3, D5, D6, D8, D9, D11, D12, D14, D15, D17, D18, D20, D21, D23=BAT85
IC1=TL081
IC2–IC5=TL084
IC6, IC7=4051
IC8=4060
IC9=TLC272
IC10=UDN2585A
IC11, IC12=LM3915

Miscellaneous:
JP1=terminal strip with 3-way jump lead
K1=audio socket
LD1, LD2=display with 5×7 matrix, e.g., Kingbright Type TC07-11EWA (larger types: TC20-11EWA; 5×8:TC24-11EWA
PCB Type 920151 (see p. 70)

Filter	f_c or f_s	Component values
IC$_{2d}$	57 Hz	R4=267 kΩ; R5, R6=249 kΩ; C1=22 nF; C2=120 nF; C3=1 nF
IC$_{2a}$	113 Hz	R9=274 kΩ; R10= 11.8 kΩ; R11=549 kΩ C5, C6=18 nF
IC$_{3d}$	255 Hz	R14=324 kΩ; R15=13.7 kΩ; R16=649 kΩ; C8, C9=6.8 nF
IC$_{3a}$	577 Hz	R19=294 kΩ; R20=12.4 kΩ; R21=590 kΩ; C11, C12=3.3 nF
IC$_{4d}$	1030 Hz	R24=287 kΩ; R25=12.1 kΩ; R26=576 kΩ; C14; C15=1.5 nF
IC$_{4a}$	2940 Hz	R29=280 kΩ; R30=12.1 kΩ; R31=562 kZ; C17, C18=680 pF (polystyrene)
IC$_{5d}$	6650 Hz	C20=309 kΩ; R34=13.3 kΩ; R35=619 kΩ; R36=wire bridge; C22=not used; C21, C23=270 pF (polystyrene) Place JP1 in position B
IC$_{5a}$	13600 Hz	R39=11.8 kΩ; R40=2.37 kΩ; R41=294 kΩ C25–C27=470 pF (polystyrene)
IC$_{5b}$		R42=51.1 kΩ; R43=4.7 MΩ; C28=100 nF;

Table 1. Component values and frequencies for eight filter sections.

Calibration

Connect the meter to a point in the amplifier where a strong signal is present; this is normally the loudspeaker terminal in an output amplifier. Make sure that the amplifier is fully driven. Turn P$_1$ so that IC$_1$ is just not overdriven. If an oscilloscope is not available, connect a multimeter, set to the 10 V a.c. range, to the output of IC$_1$. If this is an inexpensive digital multimeter, use a low-frequency input signal, say, a couple of hundred hertz. Turn P$_1$ slowly till the meter reads 9.5 V r.m.s. Then, using an input signal at a frequency in the centre of the pass-band, say, 130 Hz or 340 Hz, adjust P$_2$ until the entire associated LED bar just lights. ■

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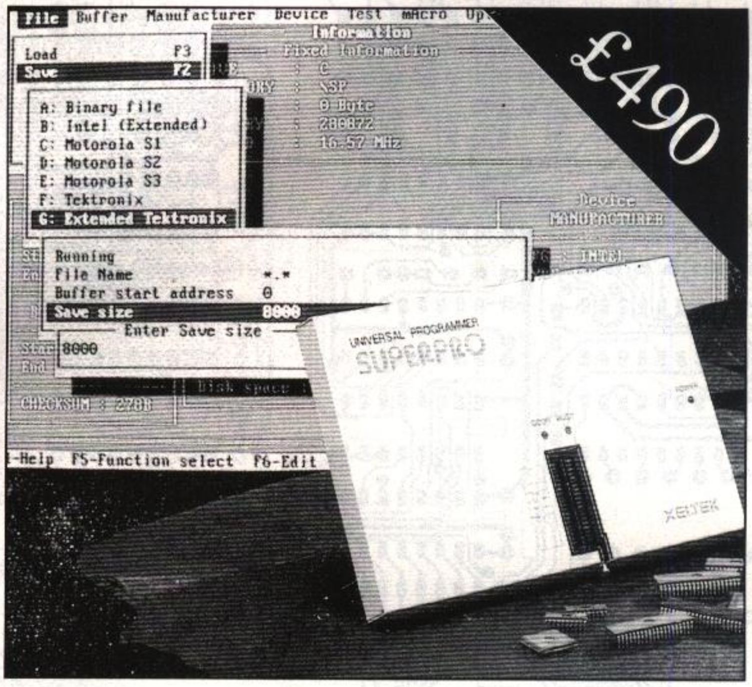

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INEXPENSIVE PHASE METER

Design by F. Hueber

The phase meter presented is based on just two CMOS ICs and a liquid-crystal display (LCD) to make it affordable with even the tightest budget.

The block schematic of the phase meter is shown in Fig. 1. Two amplifiers convert the input signal into a rectangular voltage that controls an edge-sensitive SR bistable (flip-flop). The average output of the bistable – between zero and the supply voltage – is directly proportional to the phase shift (0–360°). The measurand whose phase shift with respect to the reference signal at input B is to be determined is applied to input A. Every time the reference signal starts the positive half of its period, the leading edge of signal 1 sets the bistable. The bistable is reset when the phase-shifted signal at A starts the positive half of its period. In this way, the output of the bistable remains high longer the more the phase shift, that is, the average output voltage, increases. This is shown by timing diagrams 1 and 2 in Fig. 1.

Timing diagram 3 shows the situation when the phase shift is 0° or a multiple of 360°. In those cases, it may happen that sometimes the leading edge of input A occurs first and at other times the that of the reference signal. This will cause the output of the bistable to fluctuate between zero and the supply voltage. The meter will then give an undefined or instable reading because the average voltage cannot be exactly zero (0°) or the supply voltage (360°). This is one of the (small) prices to be paid for simplicity.

Another is that when the input signals are removed when the bistable is set, the meter reading remains at 360°. This error may be obviated by first removing the reference signal (B) and then the signal from A.

Circuit description

The two input channels are virtually identical—see Fig. 2. Only capacitors C_1, C_7 and C_9 differ from their counterparts in the other channel. These capacitors serve to synchronize the phase pattern in the two channels.

Since the two channels are near-identical, channel B only will be discussed.

The signal—input at B—is applied to the circuit via C_1, shunted by calibration capacitor C_9, which prevents direct voltage being applied to te meter. Resistor R_2 and diodes D_1 and D_2 provide protec-

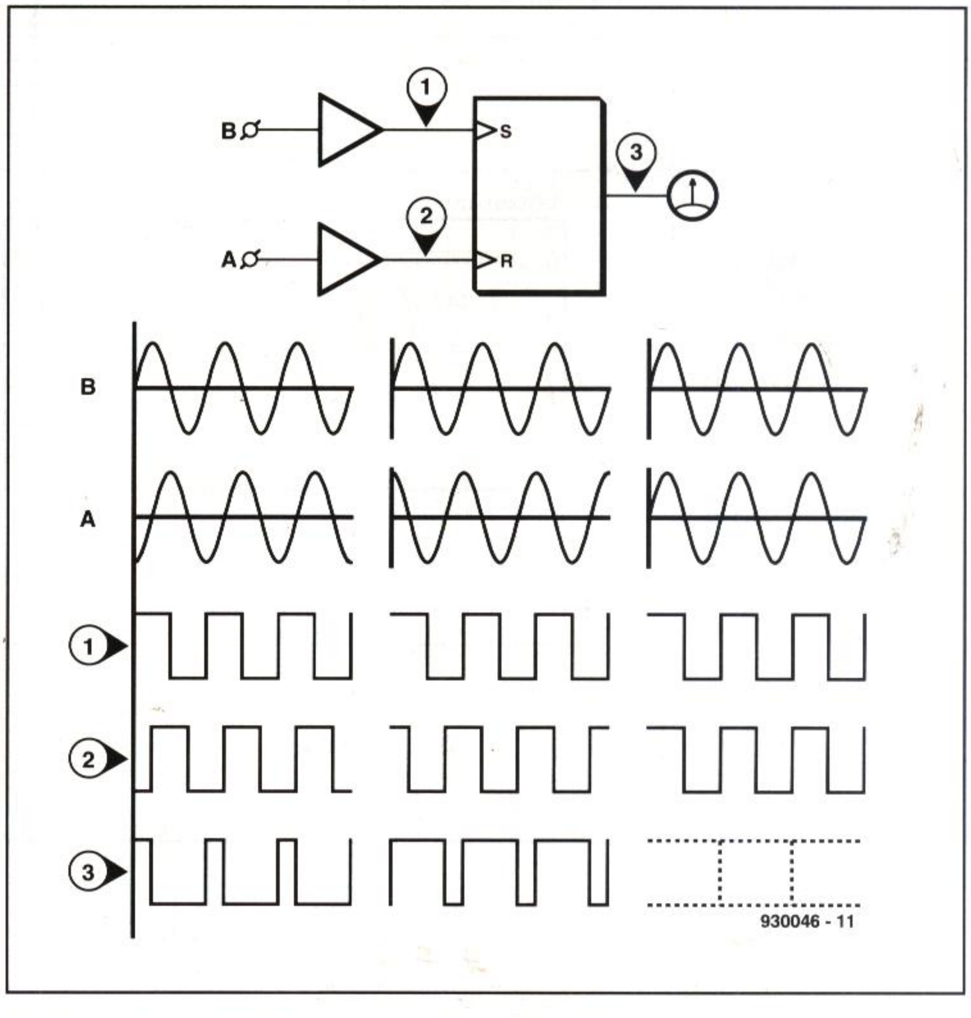


Fig. 1. The principle of the phase meter is quite simple.

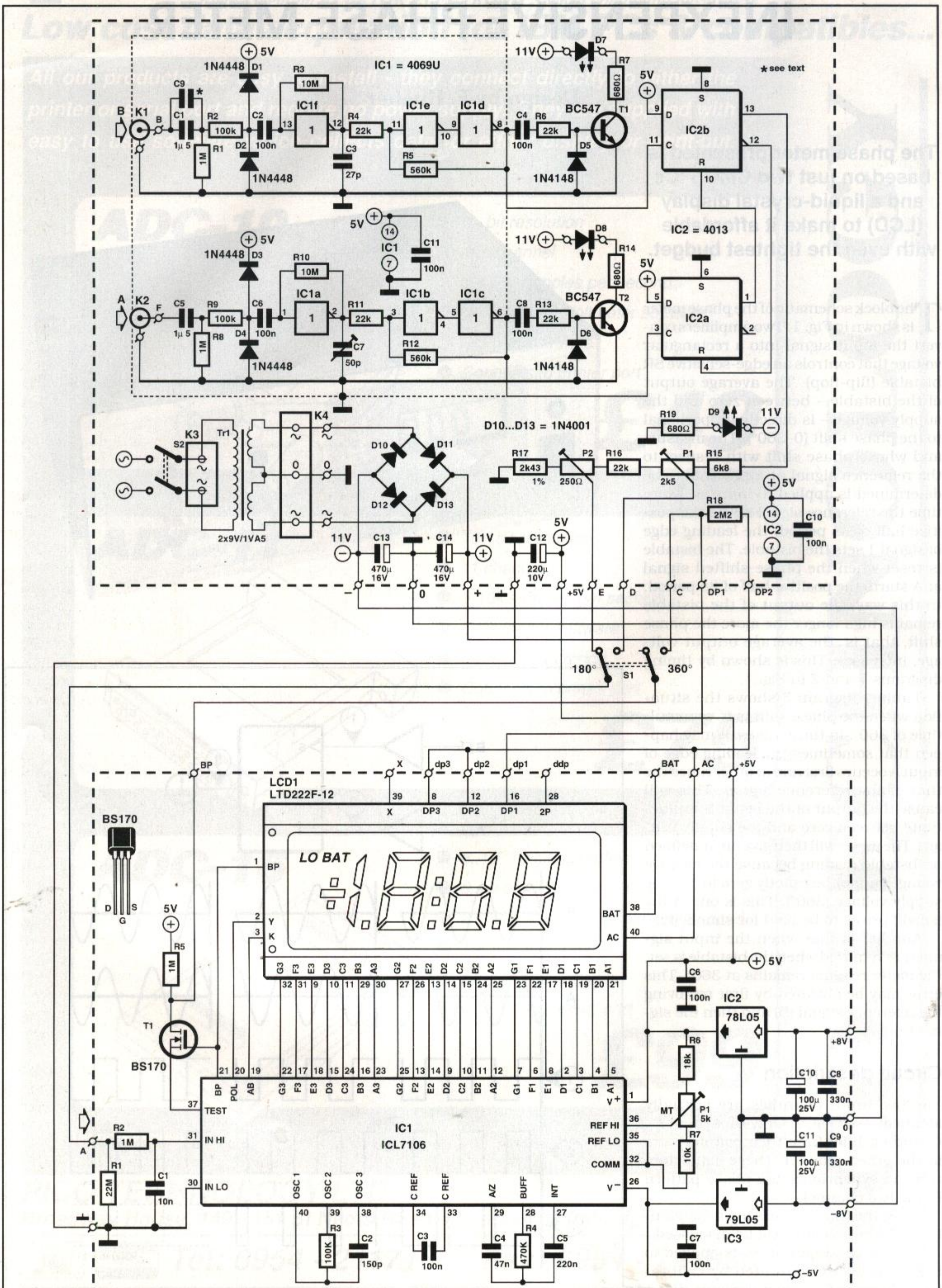


Fig. 2. Circuit diagram of the complete phase meter.

tion against too high alternating voltages at the input.

The signal is then applied to inverter IC$_{1f}$, which is not buffered, so it can be converted into a linear amplifier. In fact, IC$_{1f}$ is arranged as an inverting amplifier, whose amplification is set to about ×10 by R_2 and R_3. This arrangement is not immediately recognizable owing to the protection diodes. Capacitor C_2 prevents any direct voltage generated by the protection circuit reaching IC$_{1f}$.

In contrast to that of a standard opamp, the input impedance of IC$_{1f}$ is not easily determined. This is because of the protection circuit (which has a lower impedance at high voltages) and also since the inverter is a less ideal amplifier than an opamp. The input impedance varies between 200 kΩ and 300 kΩ, which is in most cases high enough to prevent loading of the circuit on test.

The amplifier is followed by a Schmitt trigger that converts the amplified signal to a neat rectangular signal. The trigger is formed by two series-connected inverters, IC$_{1d}$ and IC$_{1e}$ that have been provided with a measurement coupling via R_4 and R_5.

The signal is subsequently applied to bistable IC$_{2B}$ directly and to T$_1$ via C_4 and R_6. The transistor is switched on briefly at each leading edge by the charging current through C_4 and this causes D$_7$ to light. This indicates that the signal is suitable for driving the bistable. If the LED goes out or flickers, the signal is too small or something else prevents the Schmitt trigger from regular toggling.

As already stated, the difference between the two channels is confined to a couple of capacitors that enable the phase behaviour in the two channels to be identical, or nearly so, over as large a frequency range as possible. This is particularly important at the extremes of the range, because where the frequency response starts to roll-off, phase shift ensues. This does no harm as long as the shift is the same in both channels and this is ensured by the calibration points.

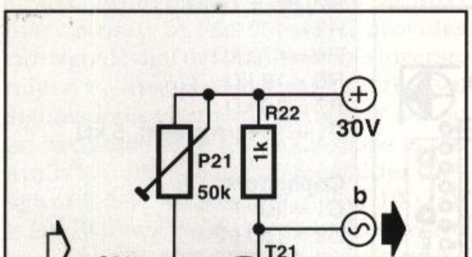


Fig. 3. Auxiliary circuit for calibrating the phase meter.

The lower cut-off point is determined by the input circuit. Since the value of capacitors normally has a greater tolerance (usually 20%) than that of resistors, capacitors are used for calibrating. To that end, C_1 may be shunted by C_9, which compensates small differences in value between C_1 and C_5 (C_1 and C_5 are compared and the smaller is fitted as C_1).

The upper cut-off point is determined primarily by parasitic capacitances in the inverters, but also by the small differences in the switching thresholds of the Schmitt triggers (bear in mind that the resistors have a tolerance of about 5%). The latter effect is particularly noticeable at high frequencies. The overall effect is compensated by C_3 and C_7.

The SR bistable is not a standard component, but is composed of two D-type bistables with reset input, IC$_{2A}$ and IC$_{2B}$. The D-bistables are interconnected in such a manner that every time one of them is set (the D inputs are permanently high), the other is reset. Just as the usual edge-triggered SR bistable, the present one has a non-permitted state and this occurs when two leading edges appear simultaneously. In that state, it is impossible to say whether the circuit interprets this as a set or a reset. This is the cause of the fact that, in theory, the meter has no stable null and cannot stably indicate multiples of 360° (which the meter 'sees' as 0°). This sounds worse than what happens in practice, because a few tenths of a degree are sufficient to give a stable display. Unreliable display of the phase shift occurs mainly when the frequency of the input signal is not stable (jitter).

The phase angle is displayed by an LCD that was also used for the 'inductance /capacitance meter' published last year[1]. This shows, by means of filter R_7–C_1, the average value of the output voltage of the bistable.

Owing to the sensitivity of the DVM module and the fact that two meter ranges are required, the output voltage must be lowered to a suitable level. This is done with the aid of potential divider R_{15}-R_{17}-P$_1$-P$_2$. From that divider, the signal is applied to the meter via one contact of range switch S$_1$. The other contact of this switch switches the decimal point for the least significant figure: the point is off when it is connected to the backplane signal (AC) via R_{18}; it is on when it is connected to inverted backplane signal (BP).

The power supply uses the voltage regulators in the DVM module. Thus, the output of the mains transformer is taken from the transformer board to the phase meter where it is rectified and buffered and then applied to the regulators in the DVM module, which hold the voltage steady at ±5 V. That voltage is then returned to the phase meter board. Note that the regulators can easily cope with the 11 V unregulated input, although the connections on the DVM module state 8 V.

Since the circuit draws only a small current, it is also possible to power it by two 9-V batteries. That saves a transformer and some other components. To reduce the current even further, high-efficiency LEDs should be used. The series resistors must then be increased to 3.9 kΩ.

Construction

The printed circuit board for the phase meter and transformer is shown in Fig. 4. This board may be cut into two if, for instance, the transformer is not used. Even if the board is used as shown, it is advisable, because of the weight of the transformer, to use eight screws to fasten it. This results in a rather more rigid construction.

The input circuits must be screened along the dashed lines. The four soldering pins at the corners make this an easy operation. The lid should not be fitted until the calibration has been carried out (possible placing of C_9). It is advisable to drill a hole in the lid through which C_7 can be adjusted. Because of the screen, it is best to connect the screened wires to K$_1$ and K$_2$ at the underside of the board. This must be done, of course, before the board is fitted into the enclosure.

The values of capacitors C_1 and C_5 must be checked with a capacitance meter. The larger value should be used in the C_5 position. The difference between the two values is compensated by C_9. To start with, make the value of this capacitor the same as the difference; the optimum value can be determined during the calibration.

The PCB for the meter module is shown in Fig. 5. Start with placing the wire bridges, because at a later stage that may be next to impossible. Place IC$_1$ in a low-profile socket, so that the display neatly fits over it. In case this proves troublesome, insert an extra terminal strip into the terminal strip of the display, so that the LCD sits slightly higher.

Because of the intricate routeing of the supply lines, it is advisable to check them thoroughly and to measure the voltage at various positions after the supply has been switched on.

Strictly speaking, the LEDs should not light when the supply is switched on, but the sensitive input channels may well pick up some noise, which is then processed as 'input'. This property may be used to advantage by touching the live input terminal with a finger. If the input channels function correctly, the associated LED should light. With S$_1$ in position 180°, the decimal point before the

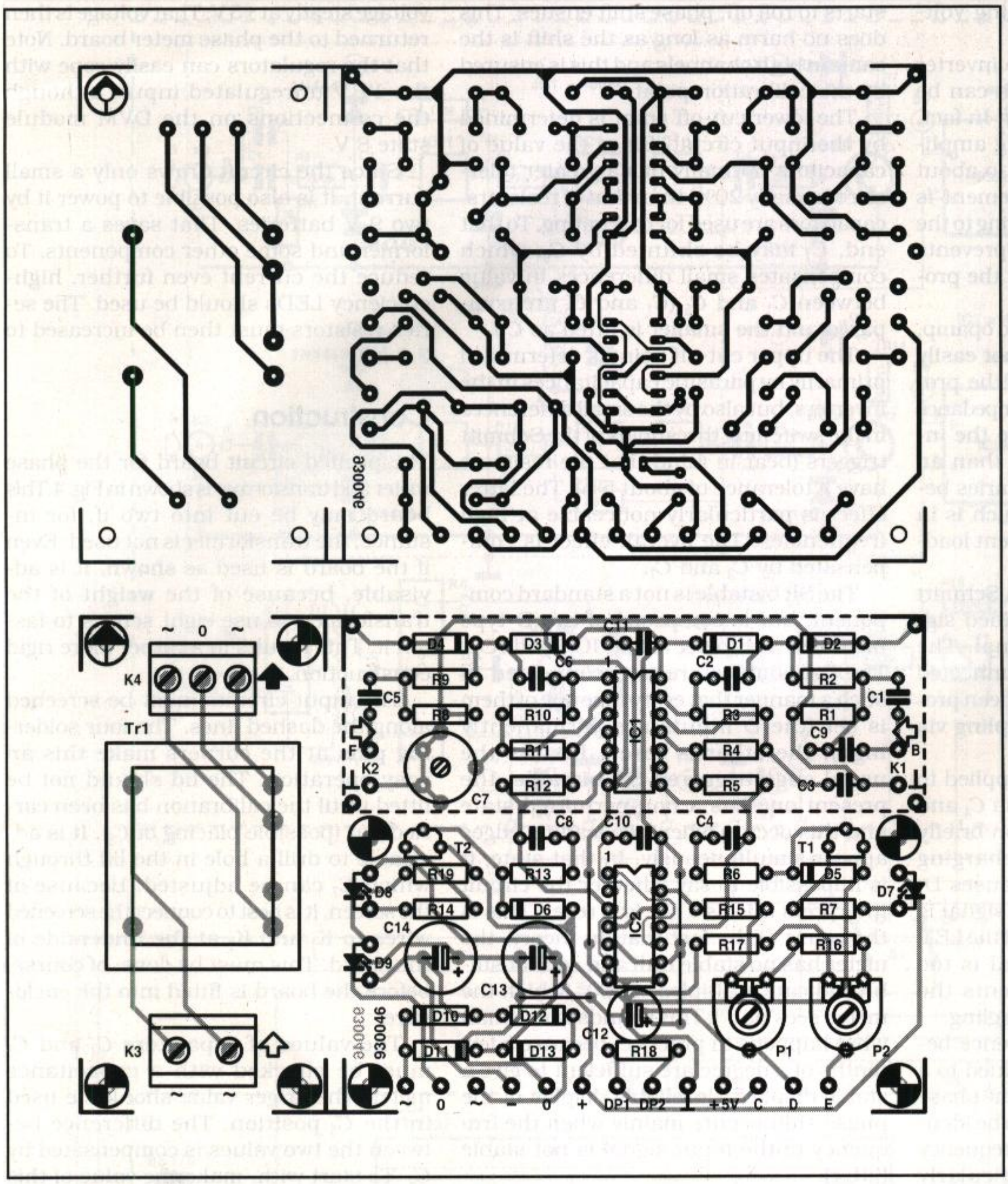


Fig. 4. Printed-circuit board for the phase meter and power supply. If necessary, the board is easily cut into two.

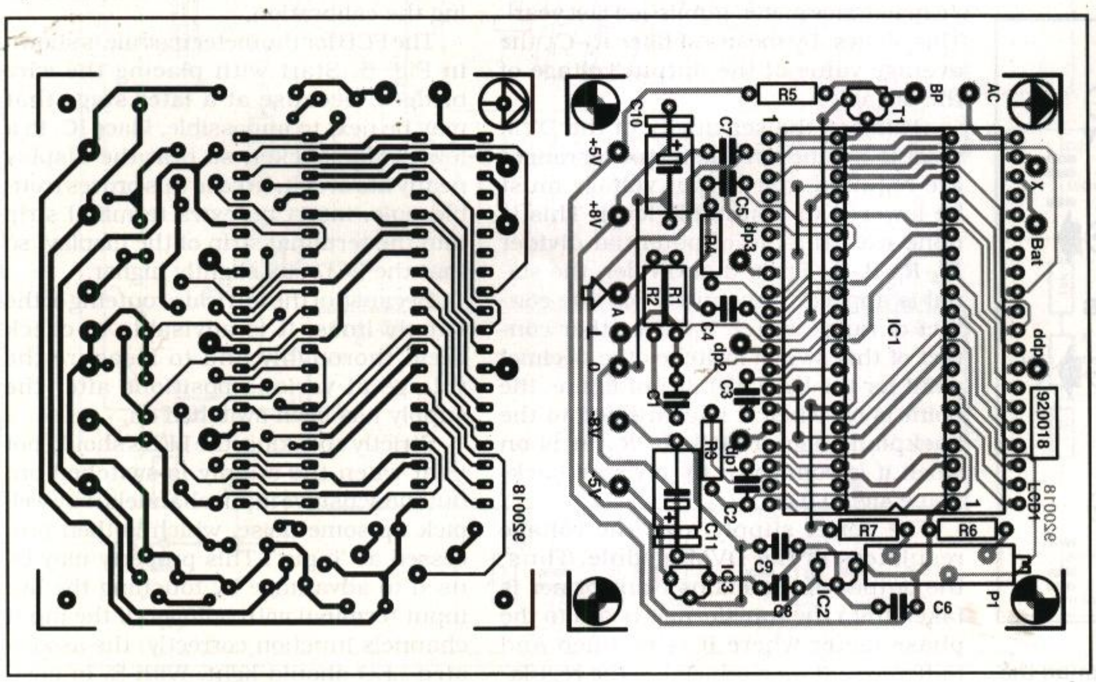


Fig. 5. Printed-circuit board for the meter module.

PARTS LIST

(Phase Meter)

Resistors:
R1, R8 = 1 MΩ
R2, R9 = 100 kΩ
R3, R10 = 10 MΩ
R4, R6, R11, R13, R16 = 22 kΩ
R5, R12 = 560 kΩ
R7, R14, R19 = 680 Ω
R15 = 6.8 kΩ
R17 = 2.43 kΩ, 1%
R18 = 2.2 MΩ
P1 = 2.5 kΩ preset
P2 = 250 Ω preset

Capacitors:
C1, C5 = 1.5 μF, MKT
C2, C4, C6, C8, C10, C11 = 100 nF
C3 = 27 pF
C7 = 50 pF trimmer
C9 = see text
C12 = 220 μF, 10 V, radial
C13, C14 = 470 μF, 16 V, radial

Semiconductors:
D1–D4 = 1N4448 or 1N4148
D5, D6 = 1N4148
D7–D9 = LED, red
D10–D13 = 1N4001
T1, T2 = BC547
IC1 = 4069U
IC2 = 4013

Miscellaneous:
K1, K2 = BNC plug
K3 = 2-way terminal block, pitch 7.5 mm
K4 = 3-way terminal block, pitch 5 mm
S1 = DPCO switch
S2 = double pole mains switch
Tr1 = mains transformer, 2×9 V, 1.5 A
Enclosure 210×80×160 mm ($8\frac{1}{4}\times3\frac{5}{32}\times6\frac{5}{16}$ in)
PCB Type 930046 (p. 70)
Front panel foil 930046-F (p. 70)

(Meter module)

Resistors:
R1 = 22 MΩ
R2, R5 = 1 MΩ
R3 = 100 kΩ
R4 = 470 kΩ
R6 = 18 kΩ
R7 = 10 kΩ
P1 = 10-turn preset, 5 kΩ

Capacitors:
C1 = 10 nF
C2 = 150 pF
C3, C6, C7 = 100 nF
C4 = 47 nF
C8, C9 = 330 nF
C10, C11 = 100 μF, 25 V, radial

Semiconductors:
T1 = BS170
IC1 = ICL7106
IC2 = 78L05
IC3 = 79L05

Miscellaneous:
LCD1 = $3\frac{1}{2}$ digit LCD
40-pin low profile IC socket
2×20-way terminal strip
PCB Type 920018 (see p. 70)

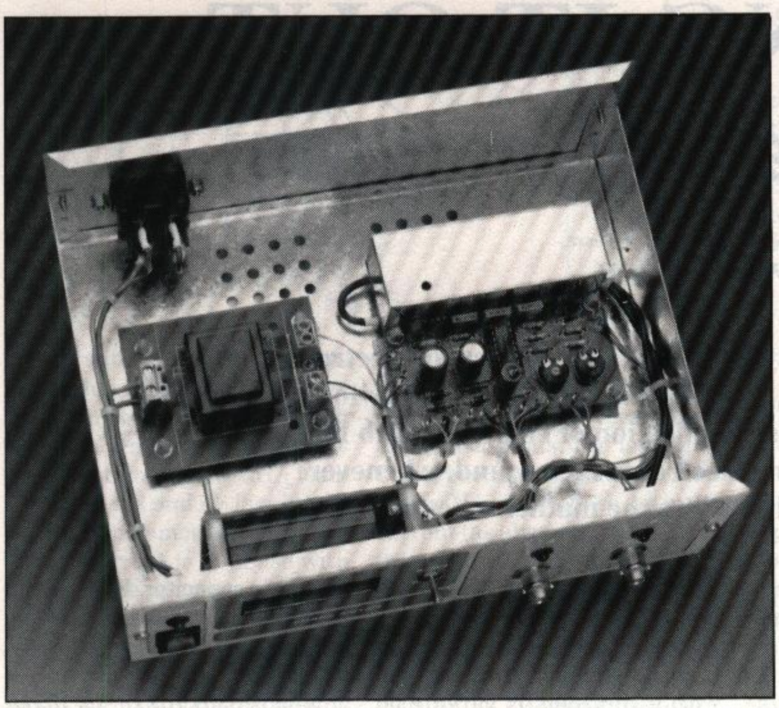


Fig. 6. Inside view of the completed phase meter.

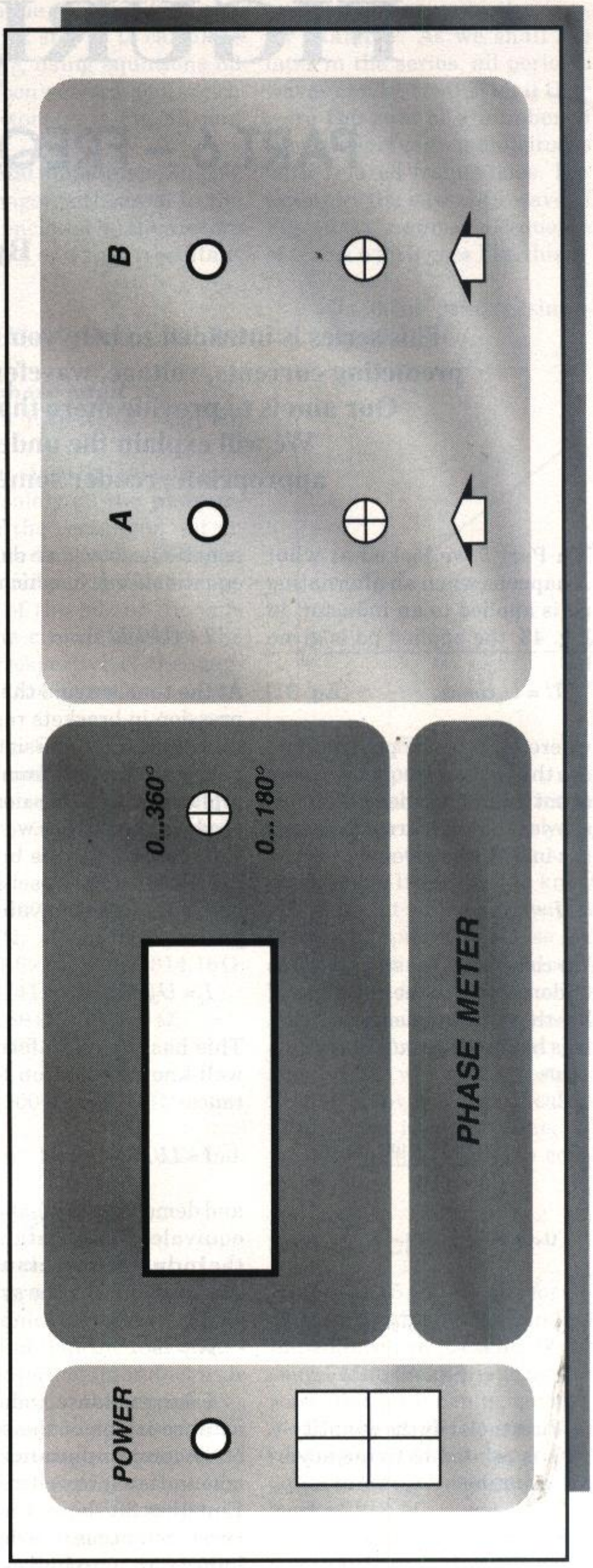


Fig. 7. The front panel foil for the phase meter is available through our Readers' services (see page 70).

last digit of the display should light. With a signal at input A (and input B short-circuited), the meter should read 0°. With a signal at input B (and input A short-circuited) and S_1 in position 360°, adjust P_1 until the meter reads 360°.

Preset P_2 (180° range) may be adjusted in a number of ways, but at all times with a 1000 Hz signal. One way is to use the 360° range as reference and to shift the signal by about 180° with the aid of an *RC* network. The preset is then adjusted until the meter readings in the 180° range and the 360° range are the same.

Another way is to use a signal source that can provide an output signal and its inverse (which is the same as one that is shifted by 180°). Again, adjust P_2 until the meter reads 180°.

A third method makes use of the auxiliary circuit in Fig. 3, which provides two signals that are one another's inverse. Adjust P_{21} in such a manner that the two signals look identical (or nearly so) on an oscilloscope. If an oscilloscope is not available, set P_2 to obtain an emitter voltage of 8.5 V. An input signal of 100 mV is fine. With the auxiliary circuit connected to the phase meter, adjust P_2 for a meter reading of 180°.

To determine the optimum value of C_9 and to adjust C_7, either a signal source with inverted outputs or the circuit of Fig. 3 is required.

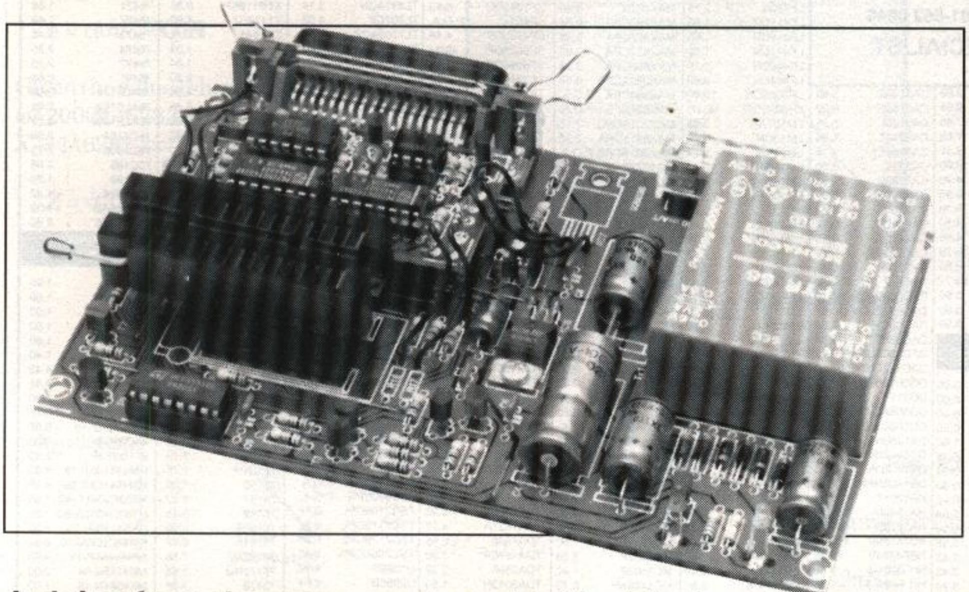
Start with lowering the frequency to between 100 Hz and 50 Hz. If everything is all right, the indicated phase angle (S_1 in position 180°) should not change by more than a few tenths of a degree. If it is more, the value of C_9 must be made a little lower or higher (this has to be tried out). Do the same with a frequency of 30 Hz. Then, adjust C_7 until the meter reads 180° again. If C_7 cannot be made small enough, the value of C_3 must be increased slightly. If C_7 cannot be made large enough, shunt C_3 with a small, say, 27 pF, capacitor.

Finally, carry out these tests at a few different frequencies to make sure that everything works all right. Readjust the relevant controls where necessary. Put the lid on the screening of the input circuits and close the enclosure. [930046]

References

1.'Inductance-capacitance meter', *Elektor Electronics*, March, April 1992.

GAL PROGRAMMER UPGRADE



Judging from the response to an *Elektor Electronics* article last year describing a low-cost GAL programmer, it looks like many of you have recognized the power of GALs, and have started programming these interesting devices. This article answers many readers' requests for a hardware extension plus upgraded software that allows more GAL types, including the industry standard 22V10, to be programmed.

Design by M. Nosswitz

AFTER some research into the programming algorithms of a number of relatively new GALs, the designer found out that only very small modifications were required to the original GAL programmer (Ref. 1) to enable it to handle even more GAL types.

The differences in GAL programming algorithms often concern the programming voltage and the signal timing. Hence, the two main programmer upgrades are (1) a variable programming voltage source and (2) modifications to the control software to implement the (complex) timing of the programming signals, and the variable programming voltage. The software automatically adapts to the GAL type in question, hence changes to the programming algorithms are transparent to the user.

In addition to GAL types 16V8(A) and 20V8(A), the upgraded GAL programmer is also capable of handling the B versions of these GALs, the 22V10, 20RA10 and the GAL6001. Programming the 6001 takes about one minute, which, admittedly, is not fast, but still useful. As regards the programming ability of different GAL brands (a subject on which we have received many letters), please do remember that the GAL programmer can only handle GALs manufactured by **Lattice**, **National Semiconductor** and **SGS/Thomson**.

Hardware extension

Everyone who has successfully built the original GAL programmer should be encouraged to upgrade it with the present hardware extension. The circuit diagram shows that the extension is relatively simple. Circuits IC1 and IC2 (Type 4094s) together form an 8-bit shift register. The output of IC2 drives IC3, a digital-to-analogue converter (DAC) Type ZN426. The DAC supplies an output voltage between 0.63 V and 1.92 V, which is programmable in steps of 20 mV. The DAC output voltage is applied to IC4, a Type CA3140 BiFET opamp, which replaces the LM317 voltage regulator originally fitted in the circuit. Apart from removing the LM317 from the board, the voltage divider around it has to be changed also. Resistor R27 (270 Ω) is changed into 22 kΩ, and R26 (2.7kΩ) into 1.8kΩ. Finally, preset P1 (1 kΩ) is

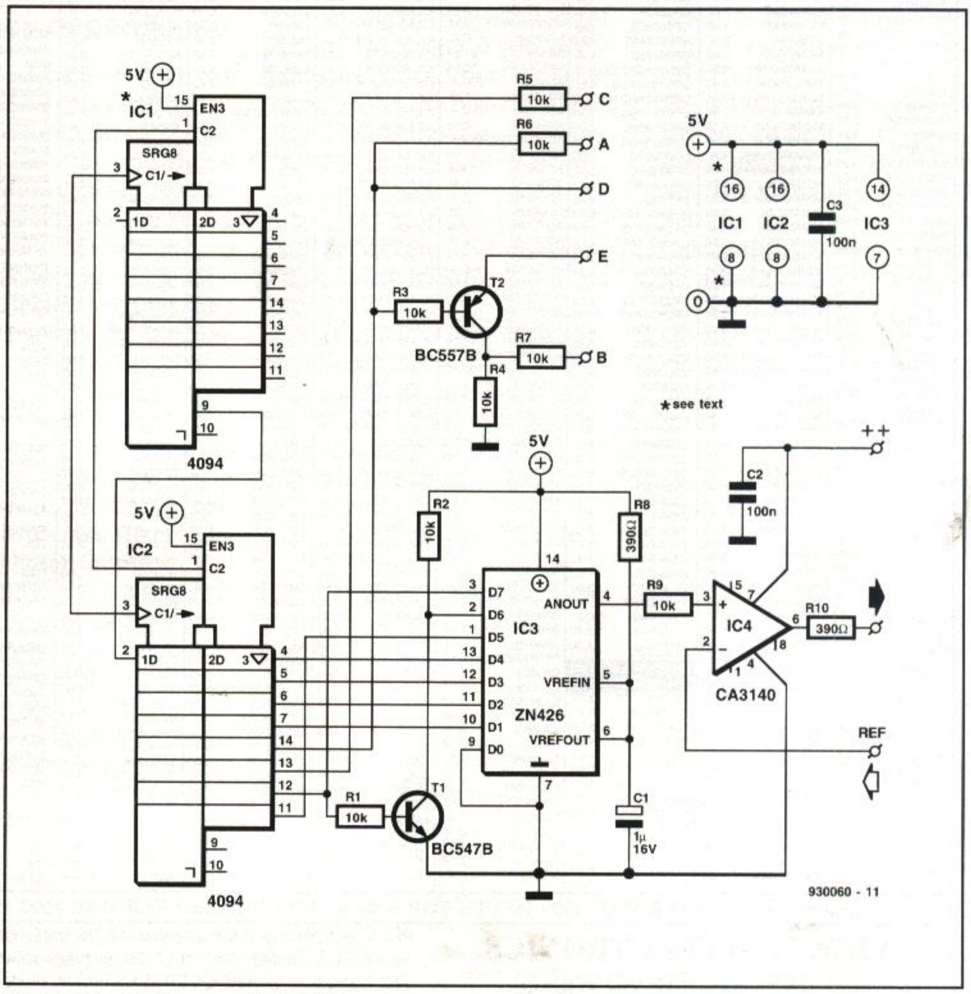


Fig. 1. Circuit diagram of the GAL programmer extension.

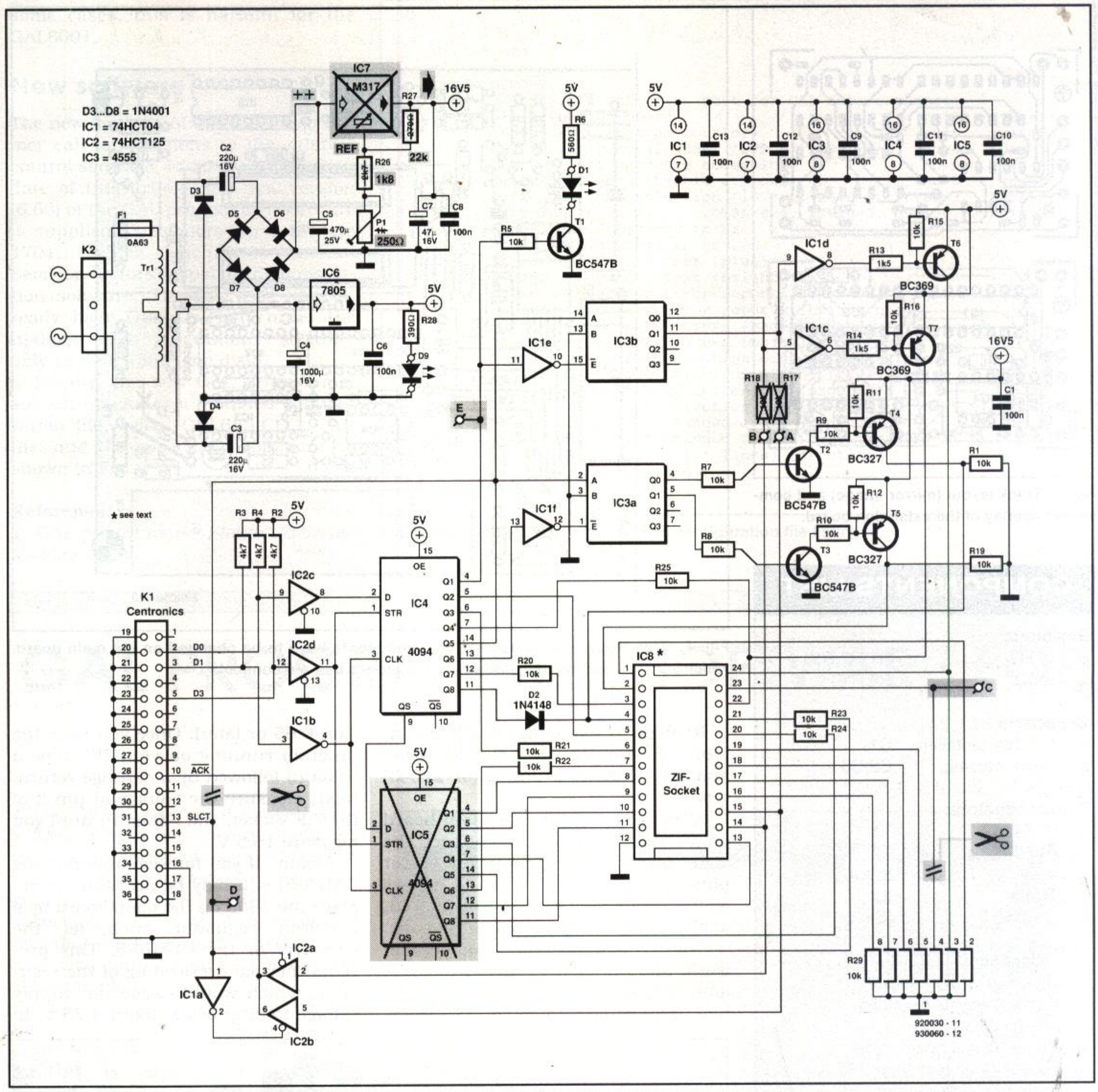


Fig. 2. This diagram shows where the original GAL programmer has to be modified to enable the extension to be integrated.

changed into 250 Ω (or 220 Ω). The opamp ensures a programming voltage range from 8 V to 23.75 V. For the sake of clarity, Fig. 2 shows the original circuit diagram with the modifications in shaded blocks.

The small board that contains the additional circuitry is fitted as an extension on to the main board. IC5 (a 4094) is removed from the main board, and replaced by the (extended) pins of the socket for IC1 on the extension board. This IC takes over the function of IC5 on the main board, and at the same time provides the connection of the supply voltage. IC2 on the extension board becomes the third element in the shift register consisting of IC4 on the main board, and IC1 and IC2 on the extension board. The third element is required to copy and latch the control word that represents the variable programming voltage. Furthermore, a number of output signals of IC2, marked A through E, are sent into the circuit. These signals are under software control, and, therefore, of little interest to the user.

Construction

As already mentioned, the extension board is plugged into the empty socket in position IC5 on the main board. The track layout and component overlay of the extension board are given in Fig. 3.

IC1 on the extension board is mounted into two IC pin rows with extra long pins, or a wire-wrap socket. The long pins are pushed through the holes in the extension board, soldered at the track side, and inserted into the socket in position IC5 on the GAL programmer main board. First, however, the extension board has to be populated. Fit eight solder pins where the wires between the extension board and the main board are to be connected. Once the extension board is complete, you can proceed with the modifications to the main board.

Remove IC7 from the main board, and solder three lengths of insulated wire in the open PCB holes. Next, re-

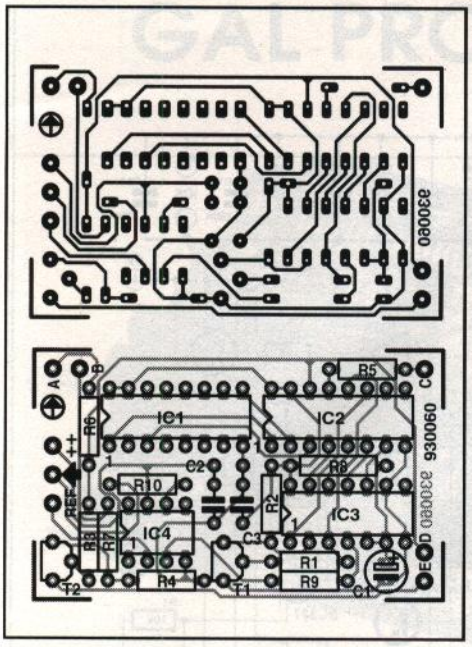


Fig. 3. Track layout (mirror image) and component overlay of the extension board.

COMPONENTS LIST

Resistors:

8	10 kΩ	R1-R7;R9
2	390Ω	R8;R10

Capacitors:

1	1µF 16V tantalum	C1
2	100nF ceramic	C2;C3

Semiconductors:

1	BC547B	T1
1	BC557B	T2
2	4094	IC1;IC2
1	ZN426	IC3
1	CA3140	IC4

Miscellaneous:

1	DIL-16 wire-wrap socket, or two 8-way IC pin strips with long pins
1	Printed circuit board, order code 930060 (see page 70)
1	Software on disk, order code 1701 or 1881 (see page 70)

move resistors R17 and R18 from the board, and solder two wires into the holes nearest R23 and R24. The next job is a little more difficult: pin 4 of array R29 has to be disconnected from the PCB, and a short wire is inserted into the hole. If you find it difficult to actually pull the array pin out of the PCB hole, you may also cut it off (using a pair of precision pliers), and pull the remaining wire out of the PCB hole (while heating it with the solder iron, of course). Next, remove the wire link between R5 and R13, and fit a wire into the hole near R2/R5. The last wire is connected to the side of R5 that is close to the wire link you have just removed.

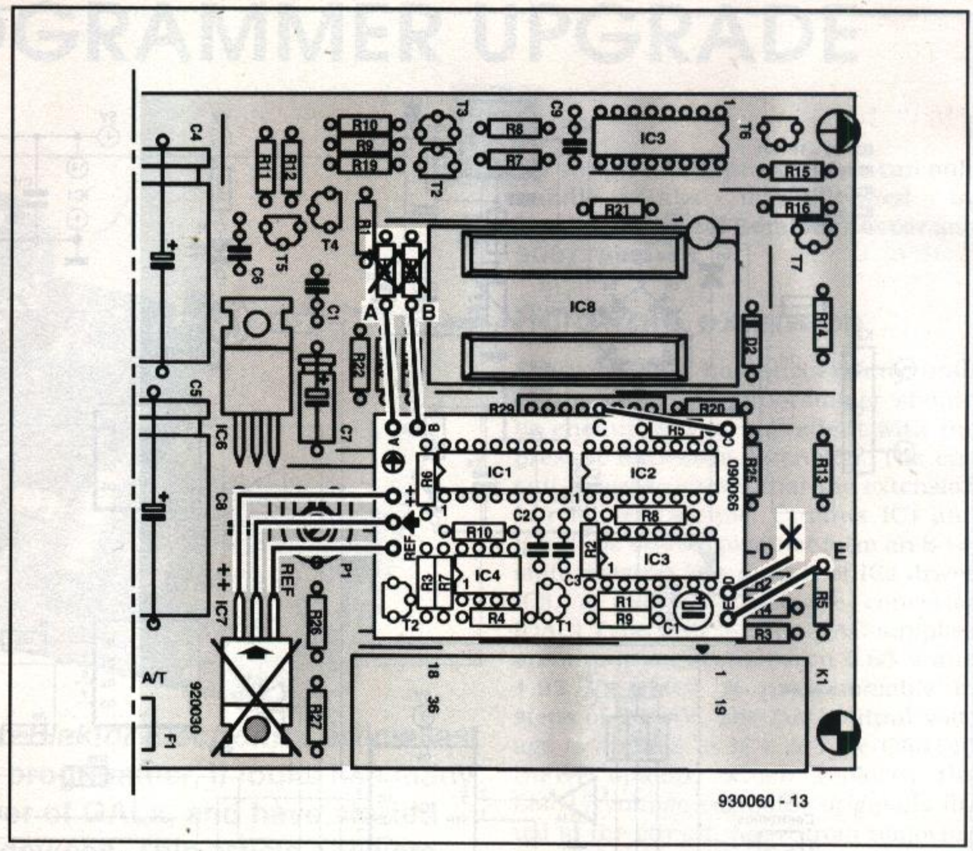


Fig. 4. This diagram tells you which components have to be changed on the main board, which wire link is removed, and where the eight wires are connected.

Replace resistor R27 by a 22-kΩ type, resistor R26 by a 1.8-kΩ type, and preset P1 by a 250-Ω (or 220-Ω) type.

After plugging the extension board on to the main board, connect the eight wires to the appropriate solder pins. The drawing in Fig. 4 shows which components must be removed, and which connections are to be made.

That concludes the modification work, and only leaves preset P1 to be adjusted, which requires the use of the new GAL programmer software (version 6.65 or later). Once you have the program running on your PC, type a colon (:) followed by a carriage return. Next, measure the voltage at pin 2 of the ZIF socket, and adjust P1 until you measure 16.5 V.

Finally, if you foresee programming GAL6001's, it may be necessary to replace the 7805 on the main board by a low-drop regulator such as the L4941BV or the L4940V5. This prevents thermal overloading of the regulator, which would cause the supply voltage to drop below about 4.75 V. In

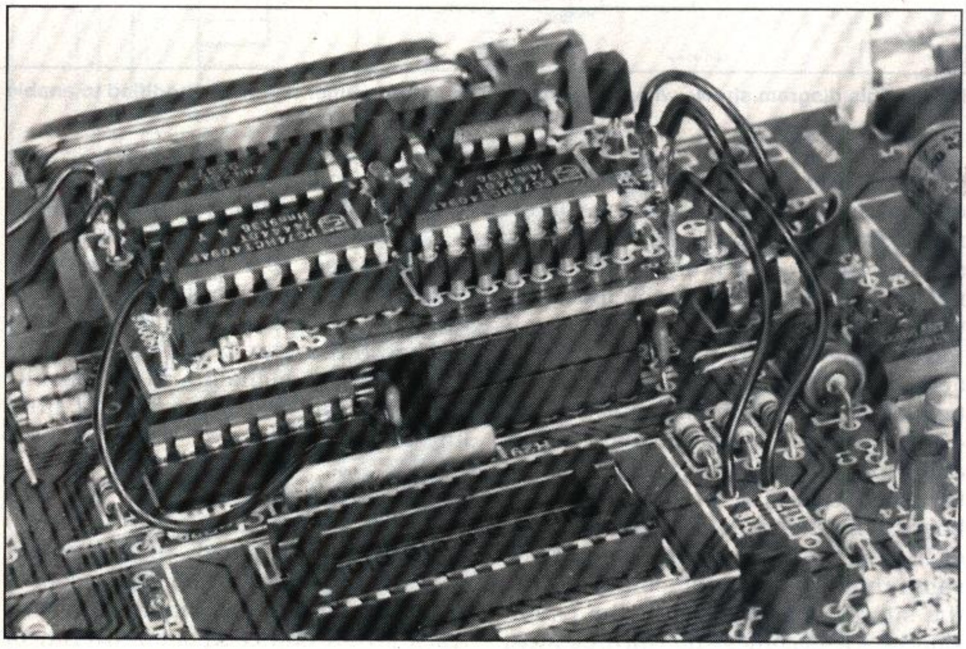


Fig. 5. Prototype of the extension board, plugged into the socket for IC5 on the main board.

some cases, this is harmful for the GAL6001.

New software

The new features of the GAL programmer call for revisions to the existing control software. From the publication date of this article, the new version (6.65) of the GAL programmer software is supplied as Readers Services item 1701, which includes National Semiconductors's Opal Jr. demonstration software. Those of you who already have Opal Jr. may order the updated GAL programmer software only as item 1881 (one disk).

Finally, the new GAL programmer software includes a modified configuration file, called GAL665.CFG. This file, and the associated comment, is shown in Fig. 6. ■

Reference:

1. GAL programmer. *Elektor Electronics* May 1992.

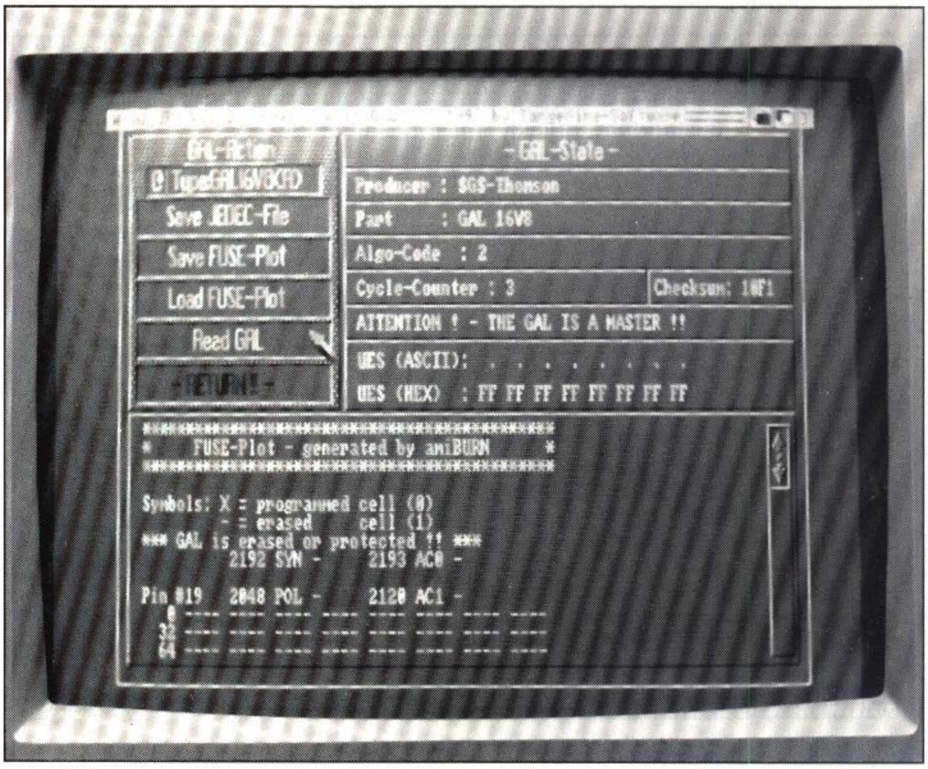
```
GAL665.cfg
(license number)
(user number)
$3bc   Address of Centronics port for GAL data exchange
1      GAL extension board                                 no=0    yes=1
1      Change PES (program counter)                        no=0    yes=1
0      Switch for general RESET (EPROM, PROM, GAL)         no=0    yes=1
1      Check if GAL hardware accessible                    no=0    yes=1
0      Select set security bit at power-up                 no=0    yes=1
1      Basic GAL type selection (16V8=1, 20V8=2, 16V8A=3, 20V8A=4,
75     beep length in ms       20V8A/B=4, 22V10=5, 6001=6, 20RA10=7)
2000   error beep frequency in Hz
2000   error display time in ms
1      Background colour Text (blue)
7      Foreground colour Text (bright grey)
5      Background colour Error reports (magenta)
7      Foreground colour Error reports (bright grey)
5      Background colour Letters (magenta)
15     Foreground colour Figures (white)
7      Background colour Selection window (bright grey)
1      Foreground colour Selection window (blue)
5      Background colour Selection bar (magenta)
14     Foreground colour Selection bar (yellow)
4      Background colour Changed cells (red)
7      Foreground colour Changed cells (bright grey)
5      Top of paper margin (in lines) (printing)
8      Left margin (printing)
```

Fig. 6. GAL programmer version 6.65 configuration file listing.

GAL PROGRAMMER SOFTWARE FOR AMIGA

SOFTWARE to control the GAL programmer is now also available for the Amiga series of computers. The Amiga software consists of two programs, AmiGAL and AmiBURN, with associated (extensive) documentation files that can be printed from disk. The disk also contains an installation instruction file.

AmiGAL is a GAL logic function editor, while AmiBURN is the actual programming software. Interestingly, AmiGAL is capable of generating JEDEC files, and has a built-in Minterms (minimal terms) generator that can help you reduce complex logic equations into a form suitable for implementation with the aid of GAL cells. AmiBURN reads the files produced by AmiGAL (or any other program capable of outputting JEDEC format files), and sets up the programming conditions required for the selected GAL. Functions like making master GALs, actuating the read protection in a GAL, device copying, producing cell hard copies, and much more, are available.



```
Producer : SGS-Thomson
Part     : GAL 16V8
Algo-Code  : 2
Cycle-Counter : 3          Checksum: 10F1
ATTENTION ! - THE GAL IS A MASTER !!
UES (ASCII):  . . . . . . . .
UES (HEX)   : FF FF FF FF FF FF FF FF

****************************************
*    FUSE-Plot - generated by amiBURN   *
****************************************

Symbols: X = programmed cell (0)
         - = erased     cell (1)
*** GAL is erased or protected !! ***
           2192 SYN -     2193 AC0 -

Pin #19   2048 POL -     2120 AC1 -
  0 ---- ---- ---- ---- ---- ---- ---- ----
 32 ---- ---- ---- ---- ---- ---- ---- ----
 64 ---- ---- ---- ---- ---- ---- ---- ----
```

AmiGAL and AmiBURN are fully menu-driven, and make full use of the Amiga's graphics power. They can be run on all types of Amiga with 512 KBytes of memory or more. Before running the software, a small hardware modification is required: pins 10 and 11 of the Centronics connector must be interconnected. Fortunately, this modification still allows the programmer to be used with a PC. The Amiga GAL programmer software may be ordered through our Readers Services as item **1841** (see page 70). ■

DIGITAL FREQUENCY READOUT FOR VHF/UHF RECEIVER

The wideband AM/FM receiver[1] described last month is not complete without a dial that tells you the transmit frequency of the station you are listening to. Such a tuning dial is described here — it takes the form of a sensitive 4-digit frequency meter with a preset option and a maximum input frequency of well over 30 MHz. Also suitable for general use in your workshop!

Design by L. Pijpers

THE circuit diagram of the frequency meter (Fig. 1) is not too complex, which is mainly by virtue of the use of an integrated counter/display driver Type ICM72117AIPI from Harris Semiconductor. The display circuit is shown separately in Fig. 2.

The function of the ICM7217AIPI is changed from a counter only into a frequency meter by IC5 and IC6d. The timebase consists of a crystal oscillator, X1-IC2, and a divider chain, IC2, IC3 and IC5. The input signal arrives at divider IC4 via a transistor preamplifier, T1. The digitized and scaled down input signal is applied to the counter IC input (pin 8) via gate IC6d, which functions as an electronic switch. IC6d is enabled during the gate time (measurement period) by pin 12 of IC5. Diodes D1-D16 serve to give to the counter a certain preset value — this will be reverted to below.

The time base pulse that controls the closing of IC6d must be accurately times to ensure the correct gate time for the counter. The timing diagram of the timebase generator, IC5, is shown in Fig. 3. The numbers 0-9 at the left of the diagram represent the Q outputs if IC5. As indicated, these outputs go high successively on each pulse applied to the clock (CLK) input. The CO (carry out) output of IC5 is high when one of the outputs Q0-Q4 is high also. The CO output is low during the rest of the time, i.e., when one of the outputs Q5-Q9 is high. This means that the CO output supplies a symmetrical rectangular signal whose frequency equals 1/10th that of the input clock signal. When the CO output of IC5 is high, IC6d is enabled, so that the count pulses arriving via T1 and IC4 are fed to the count (CNT) input of IC1. The number of pulses counted during the gate time is stored in a 4-digit counter contained in IC1.

When the gate time has elapsed, the count value is fed to the 4-digit LED display. This happens when output Q5 of IC5 goes high, whereupon IC6a supplies a 'low' to the store input of IC1.

The counter memory is cleared (reset to zero) at the start of every count cycle by a logic 'high' on Q7 of IC5, which is fed to the RESET\ input via inverter IC6b. The counter preset value defined with the aid of diodes D1-D16 is loaded into the counter when output Q8 of IC5 pulls the 'load counter' (LC) input of IC1 logic 'high'.

The input of the frequency meter is connected to prescaler output 'F' or 'G' of the Philips TV tuner in the VHF/UHF receiver. To refresh your memory, this tuner output supplies the local oscillator (LO) frequency divided by 256. The signal level is about 1 V_{pp}, which is too small to drive the digital frequency meter directly. Furthermore, the signal edges are not steep enough. These problems are resolved by the circuit around transistor T1, which acts as a preamplifier and signal shaper that turns the prescaler output signal into a neat rectangular wave with a level of 5 V_{pp}, suitable for driving the clock input of counter IC4.

IC4 divides its input signal by 2^7, which gives a total LO frequency scale factor of 2^{15} ($2^8 \times 2^7$). This means that the highest frequency at pin 13 of IC6d is about 30 kHz.

To obtain a readout in megahertz (10^6 Hz), a timebase of 1×10^{-6} s is required, which means that the period of the gate signal is 2×10^{-6} s, or 0.5 MHz. This is achieved with the aid of dividers contained in IC2, IC3a and IC3b, which scale the 8-MHz clock signal generated by the oscillator in IC2 down by a factor 2^{19} ($2^3 \times 2^1 \times 2^{15}$). Note, however, that the timebase signal is divided by 10 in IC5 before it is available at the CO output. Although this results in a display reading that is ten times too high, it increases the counter accuracy, and is simple to correct visually by lighting the decimal point on

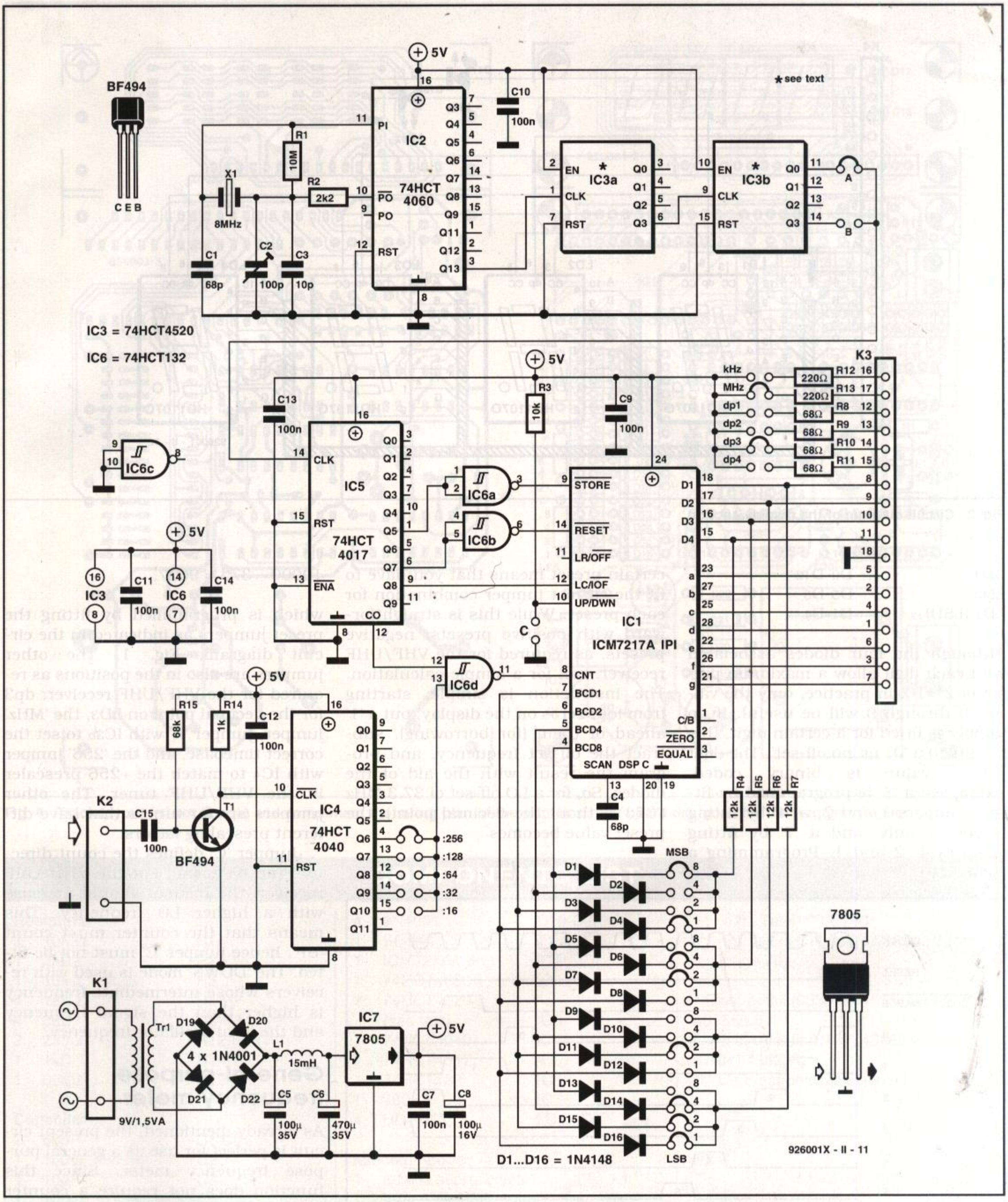


Fig. 1. Circuit diagram of the counter/power supply section. Diodes D1 through D16 serve to program a frequency off-set.

display LD3 — a simple solution, achieved by fitting jumper JP3.

Preset

When all jumpers are fitted as indicated in the circuit diagram, the frequency meter will indicate the frequency (in MHz) received on the VHF/UHF receiver. To enable the frequency meter to display the frequency of the received signal rather than that of the local oscillator, it is programmed with an off-set of 37.3 MHz. In other words, the counter's preset option must be used to subtract 37.3 from the frequency applied to its input. In practice, this is achieved by loading a preset value, which causes the counter to start at a value other than 0. The preset value has to be set separately, with the aid of diodes, for each display digit:

LD1 (MSD): D13-D16

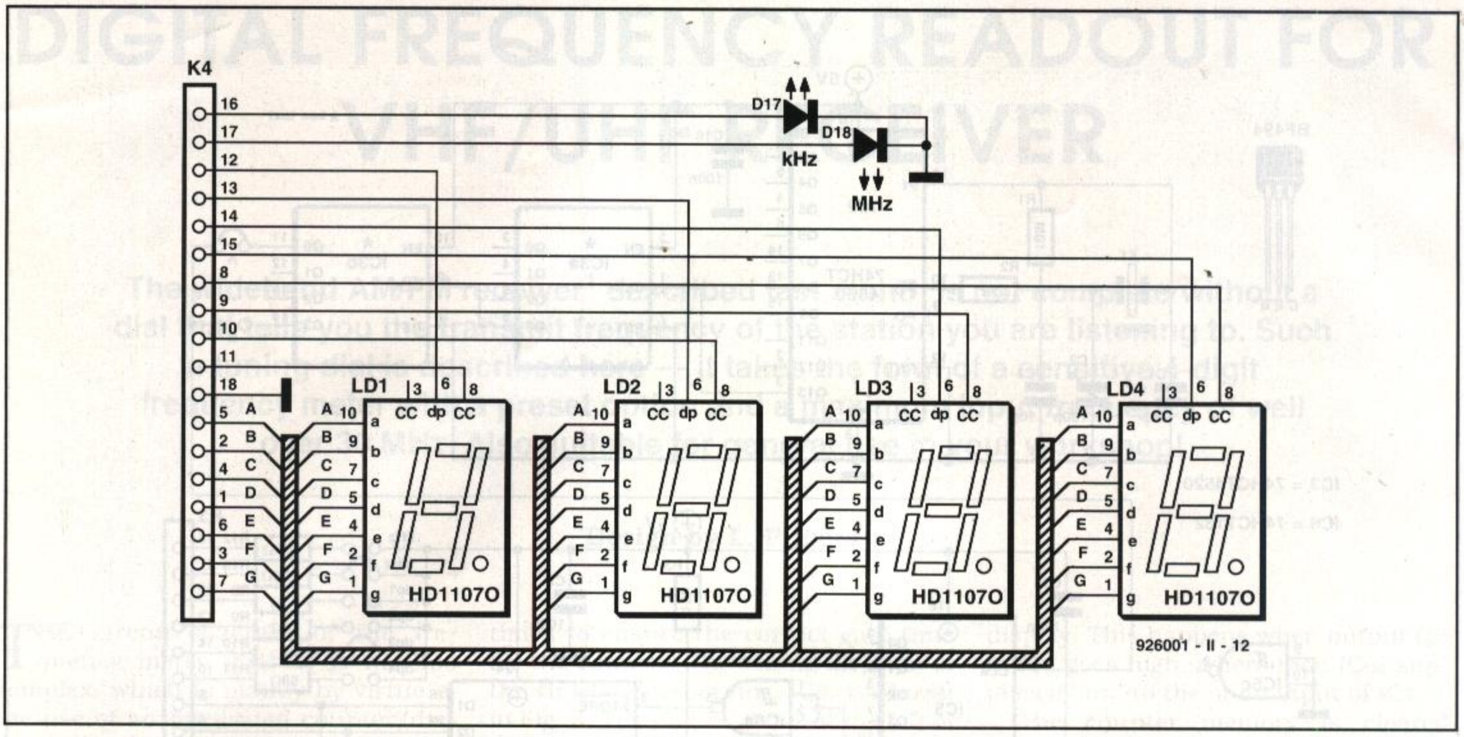


Fig. 2. Circuit diagram of the display section.

LD2	D9-D12
LD3	D5-D8
LD4 (LSD)	D1-D4

Although the four diodes associated with each digit allow a maximum preset of 2^4=16, in practice, only the values 0 through 9 will be useful. If no jumper is fitted for a certain digit, this results in a '0', or 'no off-set'. The digit preset value is binary coded. Examples: a '3' is programmed by fitting jumpers 1 and 2, a '4' by fitting jumper 3 only, and a '7' by fitting jumpers 4, 2 and 1. Programming a certain preset means that you have to fit the correct jumper combination for each preset. While this is straightforward with positive presets, negative presets, as required for the VHF/UHF receiver, call for a simple calculation. The instruction is simple; starting from four zeros on the display, put a '1' ahead of them (for borrowing), subtract the off-set frequency, and program the result with the aid of the diodes. So, for a LO off-set of 37.3 MHz ('373' without the decimal point), the preset value becomes

10000 – 373 = 9627,

which is programmed by fitting the preset jumpers as indicated in the circuit diagram, Fig. 1. The other jumpers are also in the positions as required for the VHF/UHF receiver: dp3 for the decimal point on LD3, the 'MHz' jumper, jumper 'A' with IC3b to set the correct timebase, and the '256' jumper with IC4 to match the ÷256 prescaler in the VHF/UHF tuner. The other jumpers are for tuners that have different prescaling factors.

Jumper 'C' defines the count direction (up or down). For the VHF/UHF receiver, the readout should increase with a higher LO frequency. This means that the counter must count 'UP', hence jumper 'C' must not be fitted. The 'DOWN' mode is used with receivers whose intermediate frequency is higher than the signal frequency and the local oscillator frequency.

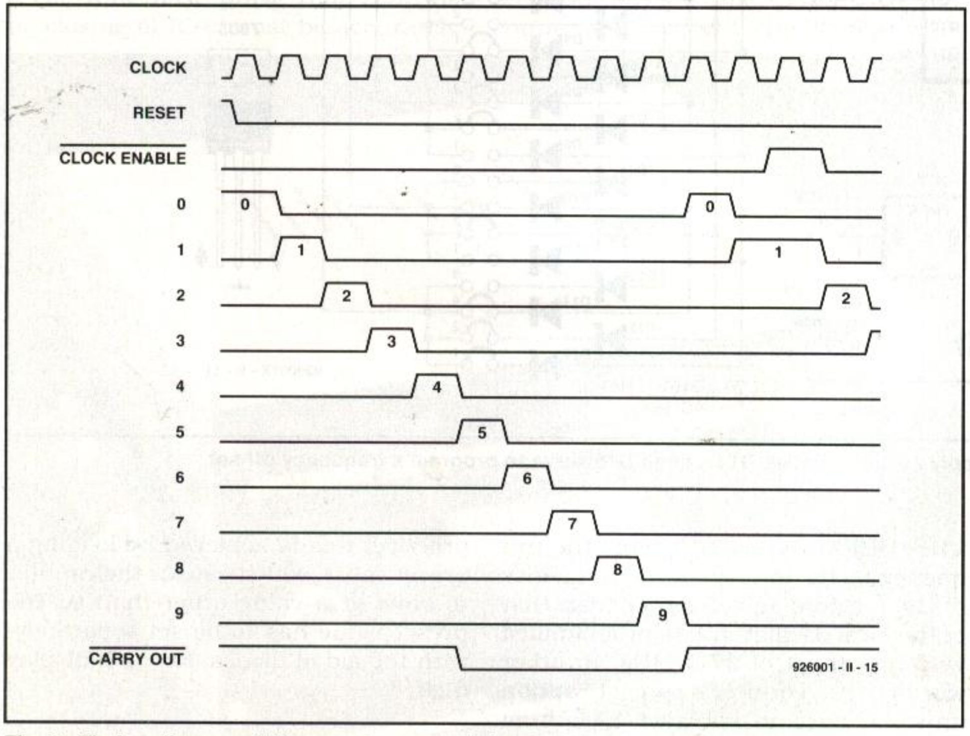


Fig. 3. Timing diagram of the counter control signals.

General-purpose frequency meter

As already mentioned, the present circuit is perfect for use as a general purpose frequency meter. Since this function does not require a counter off-set, none of the diodes D1-D16 must be fitted. Also, IC3 (a dual binary counter/divider Type 74HCT4520) must be replaced with a dual decimal counter Type 74HCT4518. No modifications are required to the printed circuit board, which is suitable for both ICs. The 4518 is virtually identical to the 4520, only the signal at output Q3 is divided by 10 rather than by 16.

For frequencies from 0.01 MHz to

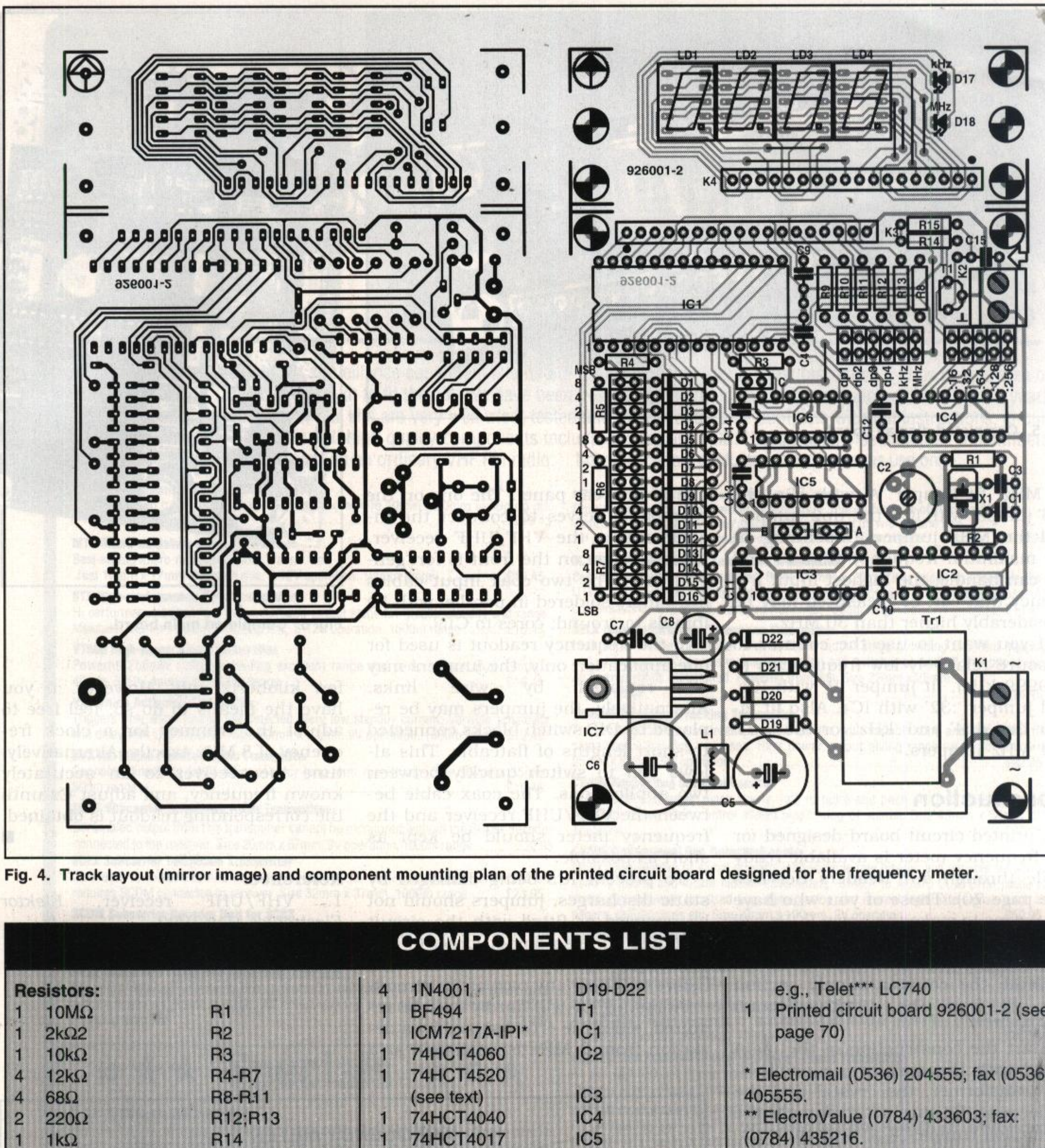


Fig. 4. Track layout (mirror image) and component mounting plan of the printed circuit board designed for the frequency meter.

COMPONENTS LIST

Resistors:

1	10MΩ	R1
1	2kΩ2	R2
1	10kΩ	R3
4	12kΩ	R4-R7
4	68Ω	R8-R11
2	220Ω	R12;R13
1	1kΩ	R14
1	68kΩ	R15

Capacitors:

2	68pF	C1;C4
1	100pF trimmer	C2
1	10pF	C3
1	100µF 35V radial	C5
1	470µF 35V radial	C6
8	100nF	C7;C9-C15
1	100µF 16V radial	C8

Inductors:

1	15mH	L1

Semiconductors:

16	1N4148	D1-D16
2	LED, red, 3mm	D17;D18
4	1N4001	D19-D22
1	BF494	T1
1	ICM7217A-IPI*	IC1
1	74HCT4060	IC2
1	74HCT4520 (see text)	IC3
1	74HCT4040	IC4
1	74HCT4017	IC5
1	74HCT132	IC6
1	7805	IC7
4	HD1107O**	LD1-LD4

Miscellaneous:

1	8-MHz quartz crystal	X1
1	9V/1.5VA PCB mount mains transformer, e.g., Monacor VTR1109	Tr1
1	double-pole mains switch	S1
1	2-way PCB terminal block, pitch 7.5mm	K1
1	2-way PCB terminal block, pitch 5mm	K2
1	18-way SIL socket	K3
1	18-way SIL header, angled	K4
1	Metal enclosure 80×150×132mm, e.g., Telet*** LC740	
1	Printed circuit board 926001-2 (see page 70)	

* Electromail (0536) 204555; fax (0536) 405555.

** ElectroValue (0784) 433603; fax: (0784) 435216.

*** C-I Electronics fax (+31) 45 241877.

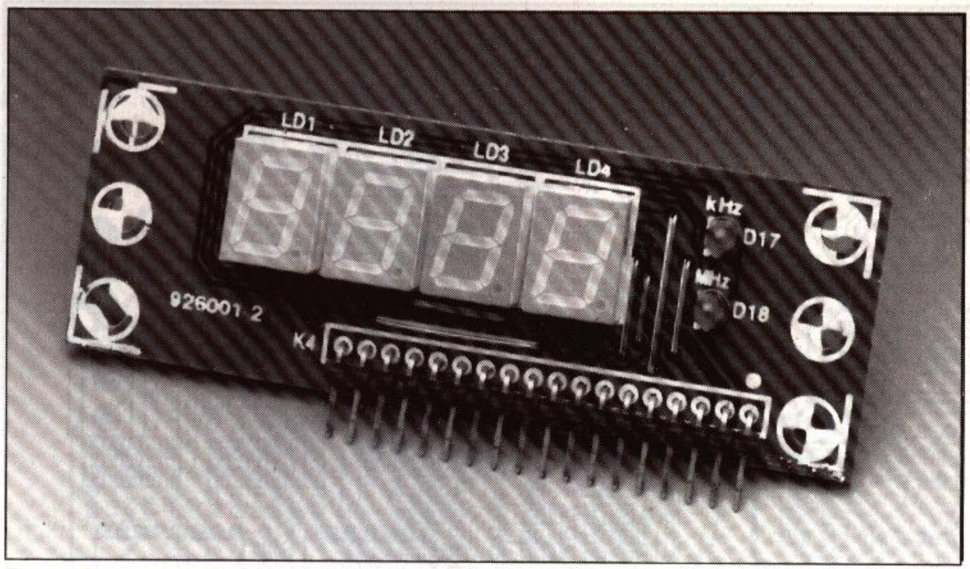


Fig. 5. Completed display board.

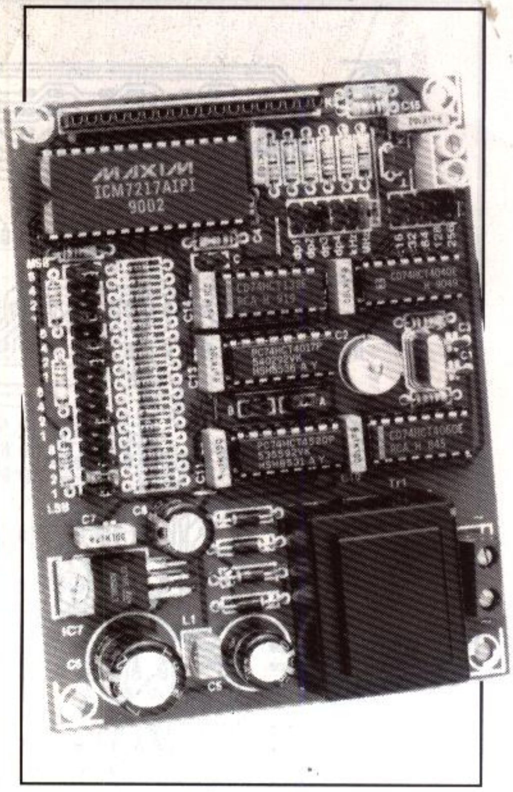


Fig. 6. Completed main board.

30 MHz, fit jumper 'A' with IC3, the ':16' jumper with IC4, the 'dp2' jumper, and the 'MHz' jumper. Depending on the maximum frequency that T1 and IC4 can handle, the highest input frequency that can be measured may be considerably higher than 30 MHz.

If you want to use the counter to measure relatively low frequencies (1 to 9999 kHz), fit jumper 'B' with IC3, and jumper ':32' with IC4. Also fit either the 'dp4' and 'kHz', or the 'dp1' and 'MHz' jumpers.

Construction

The printed circuit board designed for the frequency meter is available ready made through our Readers Services (see page 70). Those of you who have the means to make their own PCBs will find the artwork in Fig. 4. Before you start fitting parts, cut the board to separate the counter/supply section (Fig. 6) from the display section (Fig. 5).

Start the construction of the main board with the resistors, capacitors, the transformer, the crystal and the solder pins. Be sure not to damage the plastic foil trimmer (C2, near the crystal) by overheating its pins. The voltage regulator, IC7, does not need a heatsink, and may be bolted straight on to the board. As shown by the photographs of the prototype, the display board is connected to the main board with the aid of an angled pin header and a mating socket.

The completed counter/supply board is mounted on to the bottom cover of the enclosure using PCB spacers, bolts and nuts. Great attention should be paid to the insulation of the parts, wires and terminals that are at mains potential. Also be sure to use a properly rated dual-pole mains switch.

The prototype has two 50-Ω BNC input sockets — one on the front, and one of the rear panel. The one on the rear panel serves to connect the instrument to the VHF/UHF receiver, while the one on the front is for 'general use'. The two coax input cables are simply soldered in parallel with K2 (braids to ground; cores to C15).

If the frequency readout is used for one application only, the jumpers may be replaced by wire links. Alternatively, the jumpers may be replaced by DIP switch blocks connected to short lengths of flatcable. This allows you to switch quickly between two applications. The coax cable between the VHF/UHF receiver and the frequency meter should be kept as short as possible.

To prevent IC5 being damaged by static discharges, jumpers should not be removed or fitted with the circuit switched on. Also do not forget to discharge yourself (by touching the case) before touching any part of the circuit.

Adjusting C2 will hardly ever be required, since the error caused by a deviation from 8 MHz is negligible at a few kilohertz only. However, if you have the means to do so, feel free to adjust the trimmer for a clock frequency of 8 MHz exactly. Alternatively, tune the receiver to an accurately known frequency, and adjust C2 until the corresponding readout is obtained. ■

Reference:

1. VHF/UHF receiver, *Elektor Electronics* May 1992.

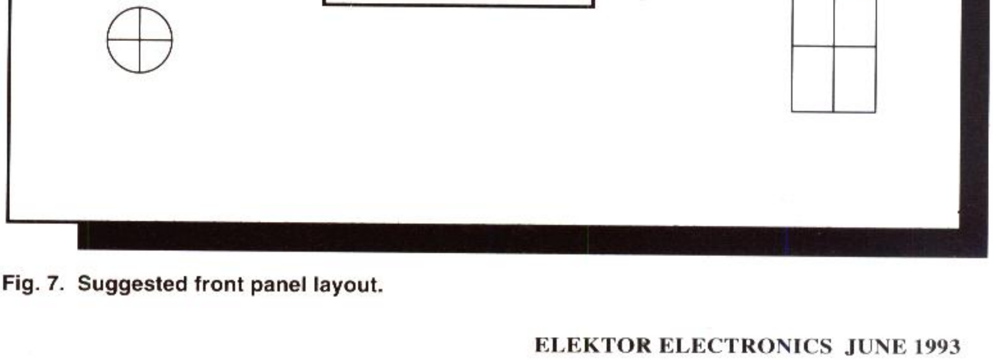
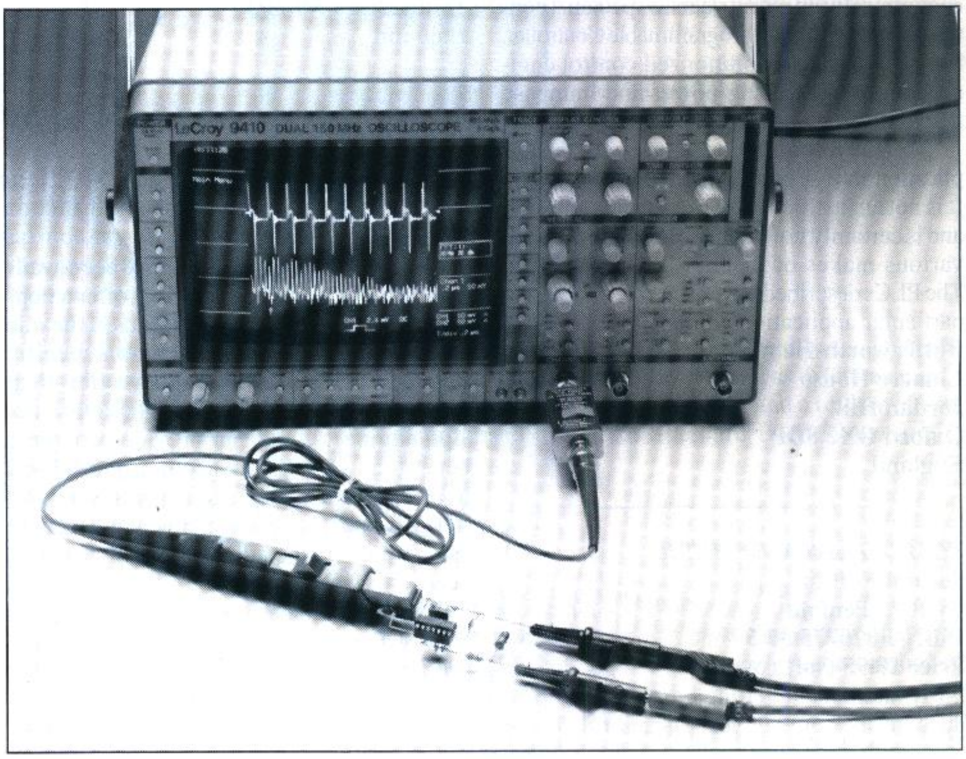


Fig. 7. Suggested front panel layout.

ELECTROMAGNETIC COMPATIBILITY (2)

From theory to practice

By J. Ruiters



As already stated in Part 1 of this two-part article, the EMC Directive must be taken into consideration when the marketing, and thus the design, specification is drawn up. This makes it far cheaper for the final product to meet the EMC guidelines than taking corrective measures in the later stages of the production process.

Although much work has been done by, for instance, the Department of Trade & Industry, The Institution of Electrical Engineers, and organizations like ERA Technology, in informing industry and all who are affected by the Directive, the practical application of EMC is still in its infancy. This is mainly because of the great variety of possible compatibility problems: after all, each design is different from the next, each product may be used in a different environment. On top of that, there are specific requirements for specific systems. Here are a few guide lines for designers.

- **Design on the basis of representative models**. In other words, use models that are characteristic of reality. Too often designers take decisions on the basis of analyses on non-valid models. If, therefore, a design decision does not yield the desired effect or result, the conclusion must be that the model used was not, or only partly, correct.
- **Always consider component properties as a function of frequency**. This rule applies to the range 0 Hz to 12 GHz. For instance, in an optoisolator common-mode signals are converted to differential-mode signals; this process, in EMC terms, is frequency-dependent.

  Another example is that one metre of yellow/green earth wire (as found in mains cable) represents an inductance of 1 µH (this will be reverted to later). At 10 MHz, this gives an impedance of 63 Ω, which shows that much equipment cannot be made EMC approved by just 'earthing it properly'.

  Figure 7 shows thatthe behaviour of electrolytic capacitors is strongly frequency-dependent: above about 10 kHz, an electrolytic capacitor is no longer a capacitor, but an inductor. This fact is important in decoupling power supply lines for high frequencies.

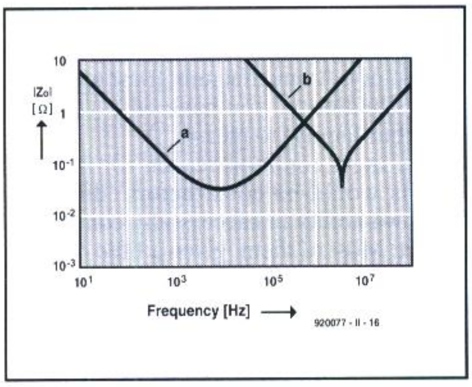


Fig. 7. Impedance as a function of frequency, (a) of a 2200 µF capacitor, and (b) of a 470 pF ceramic capacitor.

- **Think in terms of current**. It is well known that in a closed circuit current can flow even though the circuit is not connected to a voltage source. If such a circuit is placed in a varying magnetic field, a current equal to $-1/R \cdot d\phi/dt$ flows. This makes it clear that each measured potential difference (pd) is determined partly by the meter leads and the magnetic flux, $d\phi$, which (accidentally) is enclosed by these leads. It is, therefore, virtually impossible to conform to the EMC Directive on the basis of voltage considerations.

  Even a more fundamental consideration of 'potential difference' leads to a preference of thinking in terms of current. From Maxwell's Second Law, which is applicable to each and every electromagnetic phenomenon, it follows that at frequencies that are not zero the potential difference between two points is dependent on the route along which the electric field is integrated. Strictly speaking, therefore, potential difference has meaning only in the context of electrostatic fields. Note that Kirchhoff's Second Law ($\sum U=0$) is merely a special case of Maxwell's Second Law ($\sum U=-d\phi/dt$)and is, therefore, often not sufficiently accurate. However, Kirchhoff's First Law ($\sum I=0$) is always valid. In other words, voltage does not always have a rational physical meaning, whereas current does.

Properties of current

From what has been said, it is important to be well aware of a number of properties of current. In the first place: **currents always flow in closed circuits (loops)**. This is an important fact, because it is these loops that determine the emission and susceptibility to interference of an electronic circuit. It also explains why earthing does not always have the desired effect. After all, a current will flow to earth only if it cannot flow elsewhere. Mother earth is definitely not a bottomless pit into which we can dump all our interfering signals.

Each and every current sets up an electromagnetic field. A current-carrying conductor is always surrounded by a magnetic field (H), while as a result of the charge on the conductor an electric field (B) ensues between the conductor and its

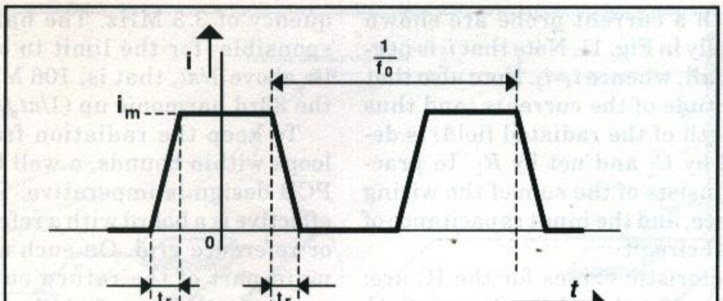


Fig. 8. True rectangular waveforms cannot be attained; the usual shape is trapezoidal as shown (slightly exaggerated).

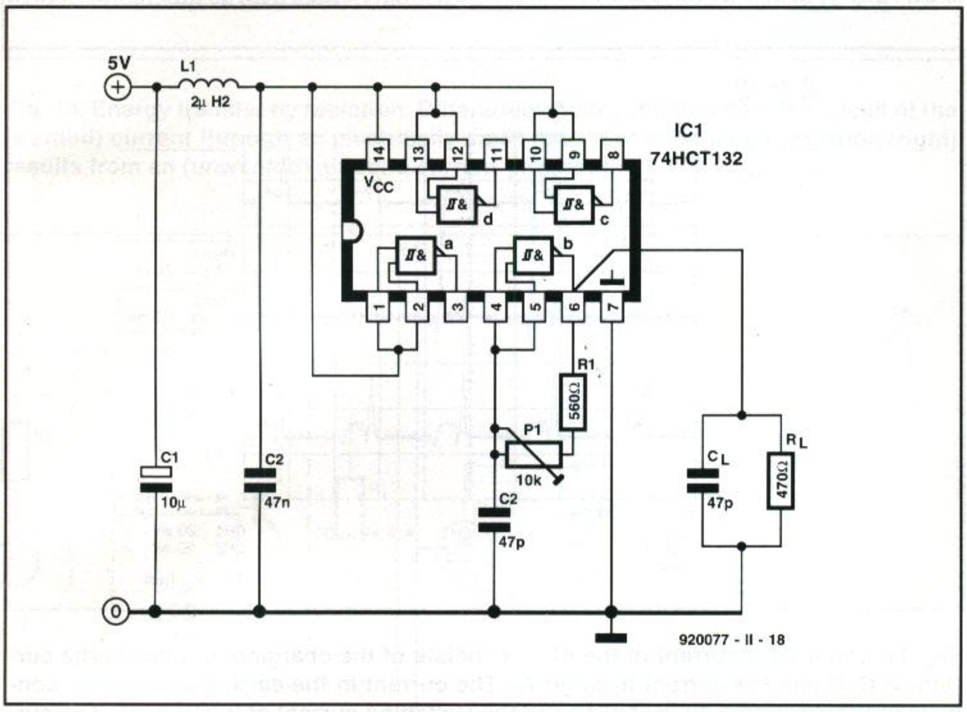


Fig. 9. In this digital oscillator, several currents have been measured. The measurement set-up is as shown in the introductory photograph.

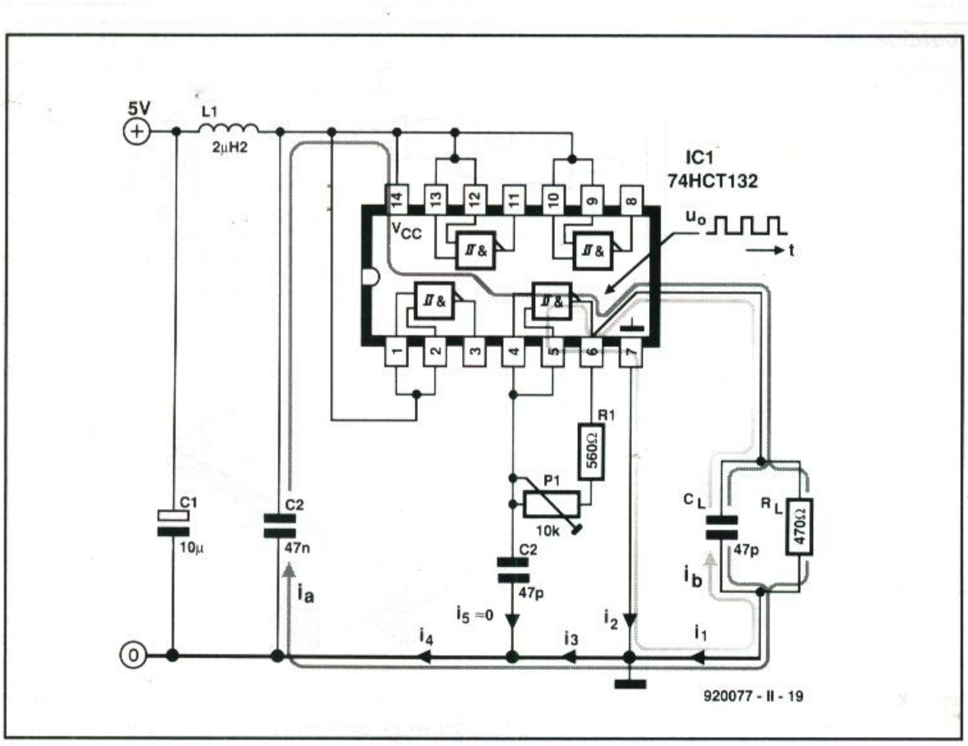


Fig. 10. The radiation of the oscillator is determined by currents i_a and i_b.

environment. The electromagnetic field causes the conductor to have not only resistance, but also several parasitic properties, such as inductance (1 nH mm^{-1}) and capacitance (read: coupling) to its ambience. The electromagnetic fields cause couplings over (electrically) short distances: cross talk.

To be able to predict the electrical behaviour of a design on the basis of a (low-frequency) network model (the CAD drawing, for instance), these field effects must be taken into account by adding to the model the correct parasitic components and sources. E-field couplings (interfaces) are indicated by parasitic Cs (important in, for instance, cross talk in high-impedance clock circuits), and H-field couplings by parasitic Ms (mutual inductance) or Ls (self inductance).

It is obvious that a knowledge of these matters is of importance in the design of printed-circuit board layouts. Many current CAD programs were written before the EMC Directive was formulated, so that, in order to comply with EMC guide lines, many critical tracks (usually about half of the total) must be laid manually by the designer.

Low and high frequency

Network theory enables the designer to approximate physical reality with models by replacing the E- and H-fields by impedances. It must be borne in mind, however, that the familiar low-frequency approximation is permitted only if the length, ℓ, of the current loop is small with respect to the wavelength $\lambda = 3 \cdot 10^8 f^{-1}$. In words, the low-frequency approximation is valid for small systems only, that is, systems that satisfy the rule of thumb $\ell \leq \lambda/10$. Even then, as has already been hinted at, a low-frequency analysis will already lose much of its value if the effects of the E- and H-fields are not, or insufficiently, specified in the network elements (for instance, because it was assumed that there are no fields around or between the connecting wires).

In the case of a large electrical system ($\ell \geq \lambda/10$), that is, a high-frequency system, the designer must apply transmission line theory (characteristic impedance, reflections, standing waves, and so on).

Designing current loops

The electric field strength around a current-carrying circuit (read: small magnetic dipole) is directly proportional to the area of the loop in which the conductive or capacitive displacement currents flow. The maximum radiated field, E_m, at a distance r from a small current loop through which a trapezoidal current flows (see Fig. 8), is estimated from:

$$E_m = 2Z_0S/\pi rc^2 f_0 i_m/t_r \qquad [\mathrm{V\ m^{-1}}]$$

where Z_0 is the radiation resistance in air (377 Ω), S is the area of the current loop, c is the speed of propagation of electromagnetic waves ($3{\cdot}10^8$ m s^{-1}), f_0 is the frequency of the trapezoidal current, i_m is the pulse maghnitude, and t_r is the first transition duration (rise time). The expression applies to a distant-field situation, which assumes that the obersver distance, $r > \lambda / 2\pi$.

The wavelength $\lambda = 3{\cdot}10^8/f$ is thus a yardstick of whether the approximation formula may or may not be used. It is important to note that λ is not the fundamental frequency, but the harmonic nearest to $1/\pi t$ Hz. This is because the electric field strength reaches its highest value with harmonics around this spectral cut-off point.

That the area, S, in the above expression must include the entire loop is made clear by considering a Schmitt trigger oscillator (see Fig. 9), which is based on a Type 74HCT132 NAND gate. The oscillator frequency can be varied with P_1 over the range 1–10 MHz.

Capacitor C_1 and low-pass filter L_1-C_2 bound the emission area in the direction of the power supply. Because of L_1, C_1, and C_2, the spectrum of the supply current (to the left of L_1) consists of low-frequency components that do not contribute to the radiation.

Because of the load on the gate, R_L-C_L, two current loops ensue that determine the radiation. The first, indicated in Fig. 10 by i_a, carries the sum of the currents through R_L, the charging current of C_L, and the switching current of the IC. The second mesh current, i_b, is characterized by the displacement current that arises as a result of C_L discharging at the instant the output of IC_{1b} goes low.

The current waveforms, i_1–i_3, measured with a current probe are shown sequentially in Fig. 11. Note that i_5 is negligibly small, whence $i_4 \approx i_3$. Note also that the amplitude of the currents (and thus the strength of the radiated field) is determined by C_L and not by R_L. In practice, C_L consists of the sum of the wiring capacitance, and the input capacitance of the digital circuit.

Characteristic values for the IC are: $t = 3$ ns, $i_m = 40$ mA and $S = 25$ cm^2. Substituting these values in the radiation formula, it is possible to estimate the maximum field to be expected at a distance of 10 m from the oscillator. From this, it appears that the radiation limit of 30 µV m^{-1} is already reached at an oscillator frequency of 3.3 MHz. The harmonics responsible for the limit to be exceeded lie above $1/\pi t$, that is, 106 MHz, or from the 33rd harmonic up ($1/\pi t_r f_0$).

To keep the radiation from current loops within bounds, a well thought out PCB design is imperative. Particularly effective is a board with a reference plane or reference grid. On such a board, the main part of the return current flows underneath the supply line (in agreement with the minimum-flux principle, this is the route of least impedance). A further benefit is that this also gives the smallest possible area of the current loop. All these measures reduce the radiation. On single-sided boards and double-sided

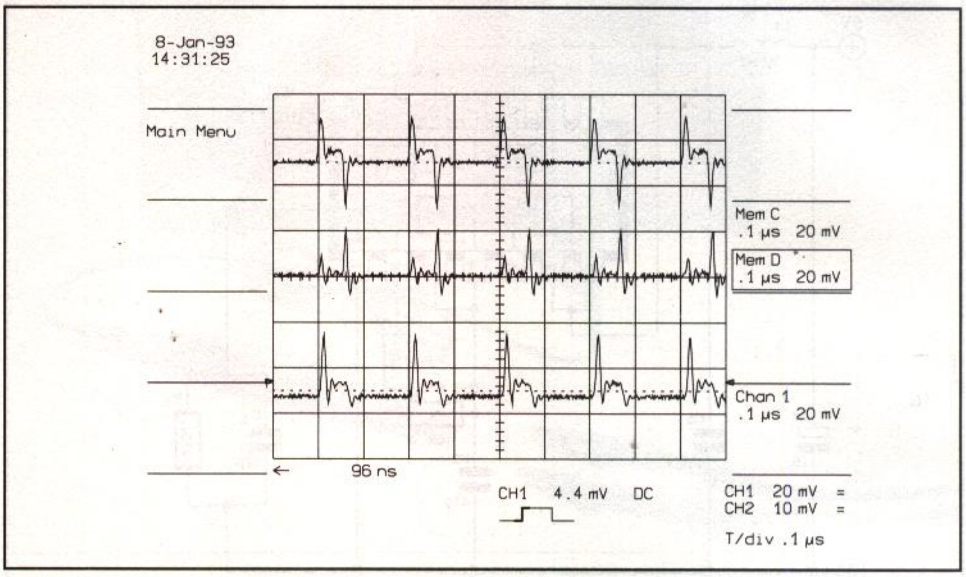


Fig. 11. The output current of the IC, 1, consists of the charging and discharge current of C_L B and the current through R_L. The current in the earth conductor, 2, consists of the discharge current of C_L and the switching current of the IC itself. The current in the large loop is equal to currents 1 and 2.

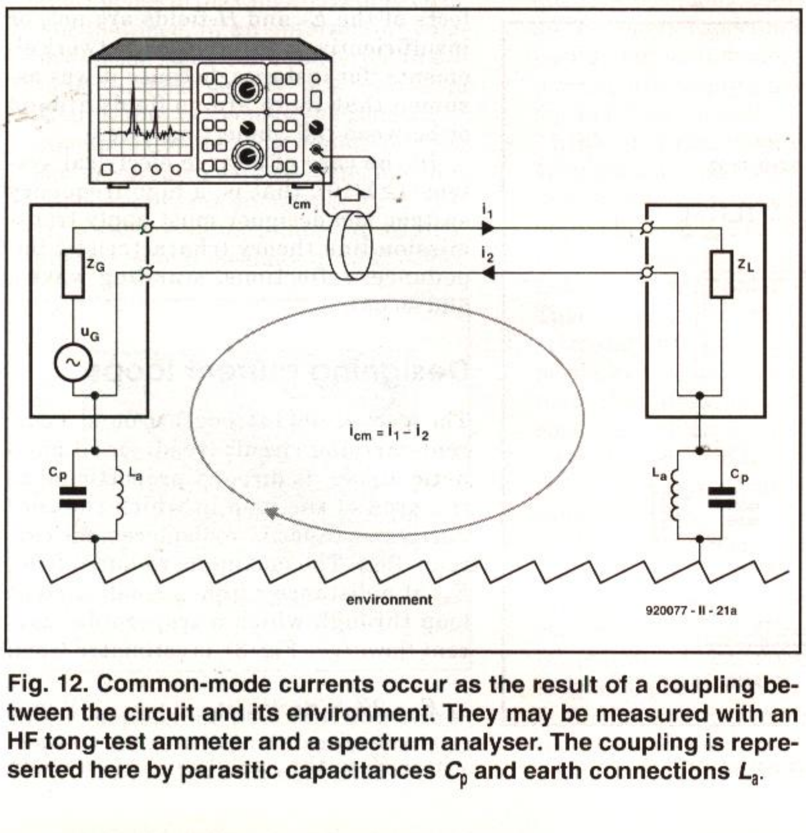


Fig. 12. Common-mode currents occur as the result of a coupling between the circuit and its environment. They may be measured with an HF tong-test ammeter and a spectrum analyser. The coupling is represented here by parasitic capacitances C_p and earth connections L_a.

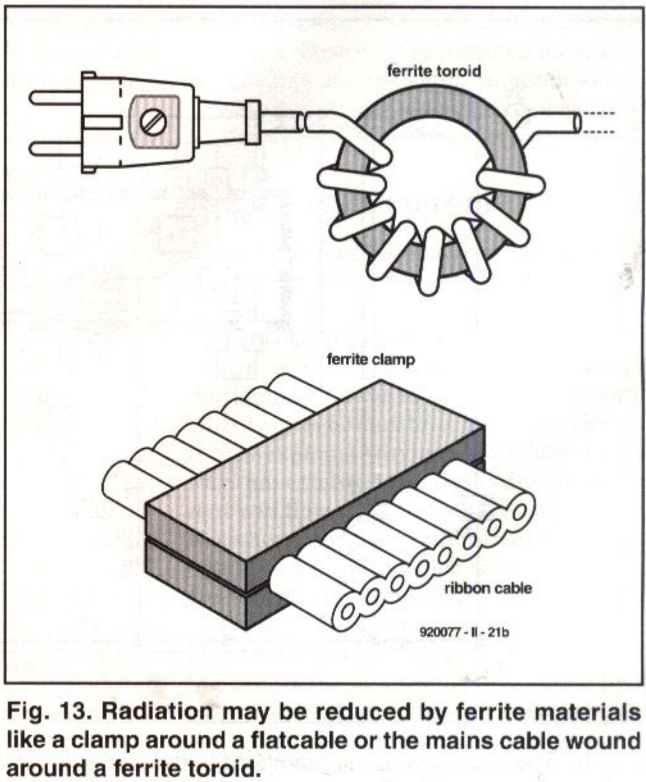


Fig. 13. Radiation may be reduced by ferrite materials like a clamp around a flatcable or the mains cable wound around a ferrite toroid.

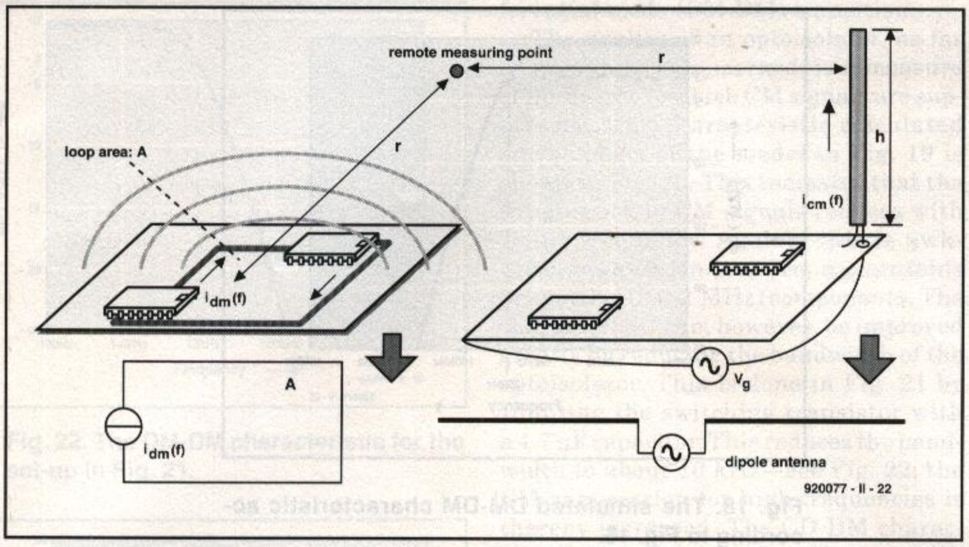


Fig. 14. Energy transfer by radiation. Differential mode radiation (left) is a result of the (wanted) current through an electrically small loop. Common-mode radiation (right) results from an (unwanted) antenna current through the cables.

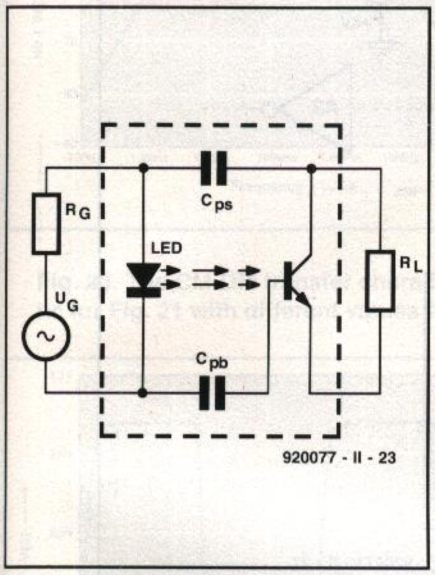


Fig. 15. Parasitic capacitances C_{pb} and C_{ps} cause the conversion in the optoisolator of CM signals into DM signals.

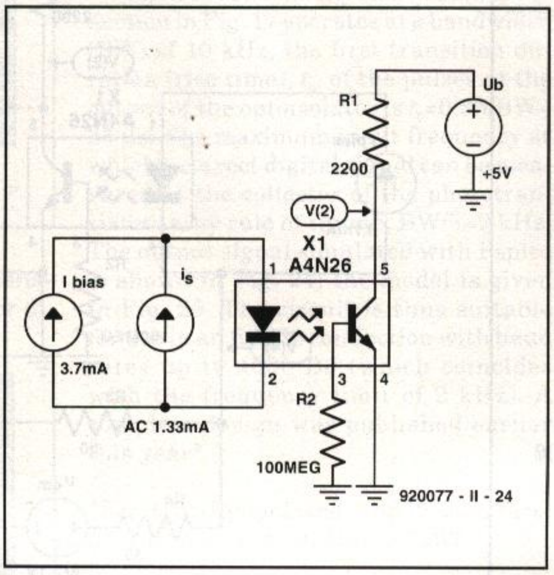


Fig. 16. Pspice model of the electrically isolated data connection in Fig. 15.

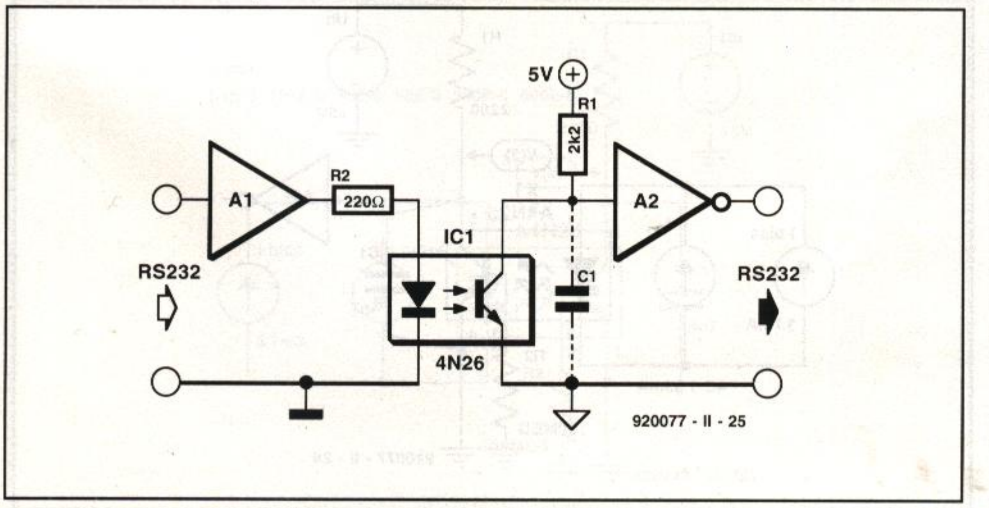


Fig. 17. Basic circuit of an electrically isolated data connection.

ones without a reference grid, the current-loop areas may be kept small by keeping the distance between the supply and return conductors small.

Also, it is advisable never to use faster logic circuits than is necessary: a higher t_r will after all cause a lower E_m. Furthermore, it is clear from the radiation formula that the clock frequency should be as low as possible. The phenomenon that E_m is directly proportional to the clock is a consequence of the fact that the amplitude of the harmonic near to $1/\pi t$ is directly proportional to f_0. Since the electric-field strength is directly proportional to the amplitude of the current, it is also directly proportional to f_0.

Beware of common-mode currents

A current loop always maintains a coupling with its surroundings, either by conduction or by radiation. ‘Surroundings’ include objects such as a metal table top, a central heating radiator, an earthing point, and so on. It all depends on which coupling predominates at a given frequency. Owing to the coupling to the surroundings, common-mode currents, also called asymmetrical currents, arise—see Fig. 12. Unfortunately, common-mode currents often flow through conductors (supply cables), whose dimension is of the same order as the wavelength: for instance, 106 MHz= 2.8 m. This means that in electronic systems whose dimensions are much smaller than the wavelength of the signals, the cables connected to the system radiate more than the tracks on the PCB. Therefore, **the radiation of most products is determined by the magnitude of the high-frequency common-mode currents flowing in the cables.**

The CM currents may be measured with an HF tong-test ammeter and a spectrum analyser. In the design stages this test and the rule of thumb $I_{CM}<5$ μA gives a good idea of whether the radiation will be higher or lower than the legal limit of 30 μV m^{-1}. If, in the prototype, the measured CM current through one of the cables (mains lead, cable to printer, signal cables) is greater than 5 μA, the final product will almost certainly exceed the maximum permissible radiation.

The radiation can be reduced by inserting a high CM impedance in the current path. For example, a ferrite clamp may be placed around a flatcable as shown in Fig. 13. The same drawing shows how the CM currents in a mains lead may be reduced by winding the lead through a ferrite toroid.

Figure 14 shows two other ways via which interference may be transferred through radiation.

Design example

An optoisolator can often be used to put some of the rules stated into practice. It is an analogue device that is frequently used with digital hardware. In such cases, the optoisolator is controlled digitally, so that, at least from a functional point of view, its output is also digital.

A suitable optoisolator for use in EMC designs is shown in Fig. 15. As usual in such a device, the signal transfer is effected by light. Capacitors C_{pb} and C_{ps} show, however, that there is another, spurious coupling between input and output. The effect of these parasitic capacitances has been investigated with a simulation program, Pspice. A setup with which this program can be used is shown in Fig. 16. This model is derived from the electrically isolated data connection in Fig. 17.

In Fig. 16, the optoisolator has been set to its linear operating range with a direct current of 3.7 mA. This value has been determined empirically and ensures that a direct voltage, whose level is equal to half the supply voltage, is present at the output. To enable the differential mode to differential mode transfer, $u_{out}/i_s = V(2)/i_s$, to be computed, an alternating current source, providing 1.33 mA,has been added at the input. With Pspice this source can be frequency-swept and the amplitude characteristic shown in Fig. 18 calculated. The most important datum to be gleaned from the characteristic is that the bandwidth for the wanted signal transfer is about 25 kHz.

In practice, the electrically isolated data connection will be affected by the common mode source of interference across the optoisolator. To study the effect of this, a voltage source, u_{CM}, and two 50-Ω impedances have been added to the model in Fig. 19. Since the optoisolator is not ideal (C_{ps} and C_{pb}), part of u_{CM} will appear at the output. This is awkward, because this interference signal is in series with the output voltage. If the level of the interference is (relatively) high, it is possible that gate A2 (read: wideband amplifier) produces erroneous logic levels during the transition from one to the other. This comes down to insufficient immunity. Note that this transition in EMC literature is called common-mode/dif-

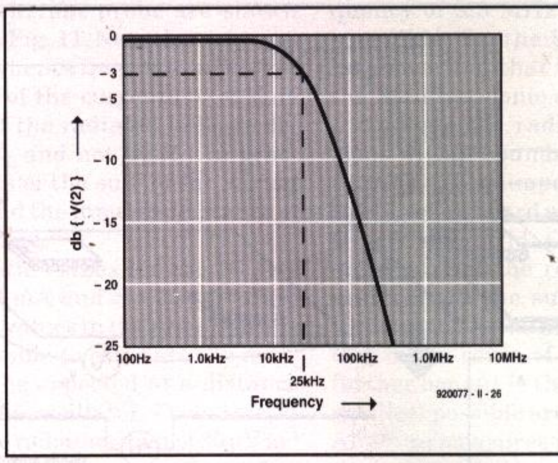


Fig. 18. The simulated DM-DM characteristic according to Fig. 16.

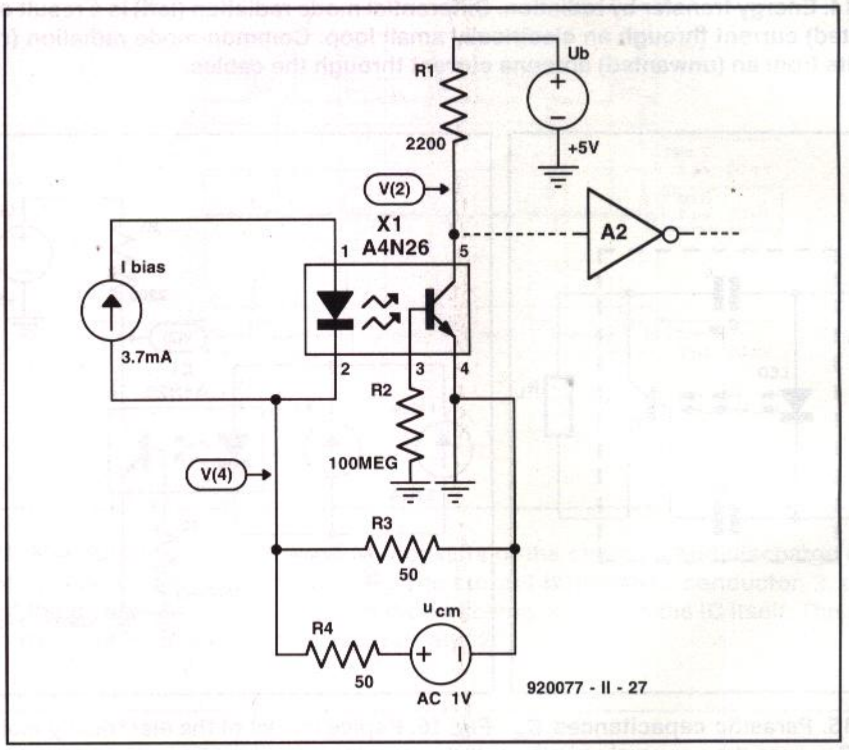


Fig. 19. To compute the CM-DM transfer, voltage source u_{CM} was added to the model in Fig. 16.

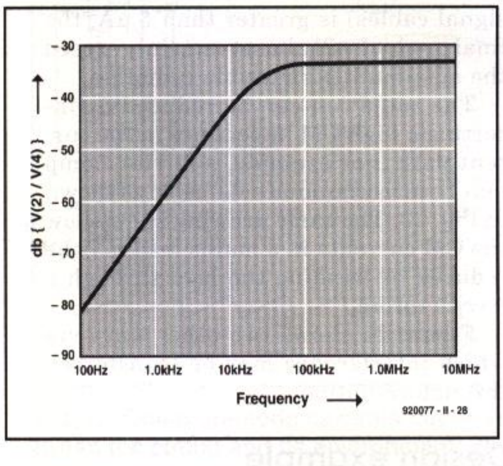


Fig. 20. CM-DM transfer characteristic computed from the setup in Fig. 19.

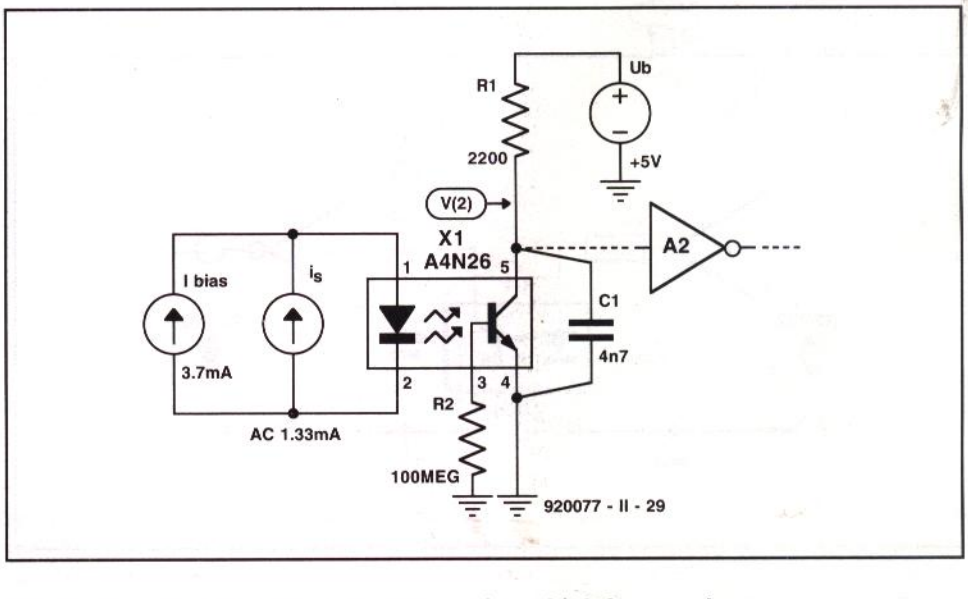


Fig. 21. Capacitor C_1 reduces theDM transfer at high frequencies.

ferential mode (CM-DM) transition.

The quality of an optoisolator, as far as immunity is concerned, is a measure of the degree to which CM signals are suppressed. The characteristic calculated on the basis of the model in Fig. 19 is shown in Fig. 20. This indicates that the suppression of CM signals reduces with rising frequency. Agains, this is awkward, because, in practice, u_{CM} contains primarily HF (>1 MHz) components. The characteristic can, however, be improved greatly by reducing the bandwidth of the optoisolator. This is done in Fig. 21 by shunting the switching transistor with a 4.7 nF capacitor. This reduces the bandwidth to about 10 kHz—see Fig. 22; the CM suppression for high frequencies is thereby increased. The CD-DM characteristic for the model in Fig. 21 with shunt capacitors of 1 nF and 4.7 nF is given in Fig. 23. It is clear from the curves that the CM suppression is inversely proportional to the bandwidth.

When the electrically isolated data connection in Fig. 17 operates at a bandwidth (BW) of 10 kHz, the first transition duration (rise time), t_s, of the pulses at the output of the optoisolator is t_s=0.35/BW= 35 µs. The maximum input frequency at which a correct digital signal can be measured at the collector of the phototransistor is, by rule of thumb, BW/5=2 kHz. The output signal simulated with Pspice is shown in Fig. 24; the model is given in Fig. 25. The circuit is thus suitable for use in an RS232 connection with baud rates up to 4000 Bd (which coincides with the frequency limit of 2 kHz). A complete design was published earlier this year*. ■

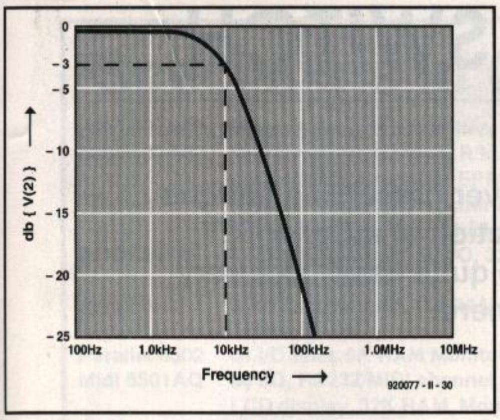


Fig. 22. The DM-DM characteristic for the set-up in Fig. 21.

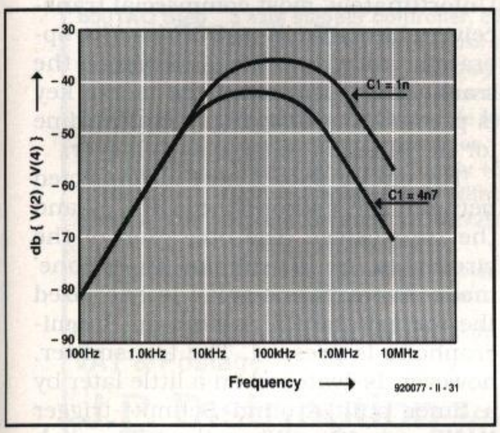


Fig. 23. The CM-DM transfer characteristic for Fig. 21 with different values for C_1.

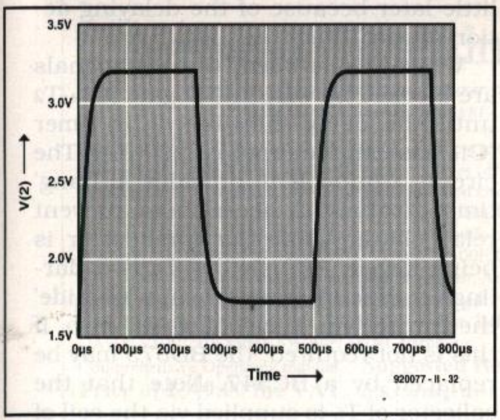


Fig. 24. Characteristic of the output voltage with a channel bandwidth of 10 kHz and a rectangular (2 kHz) input current.

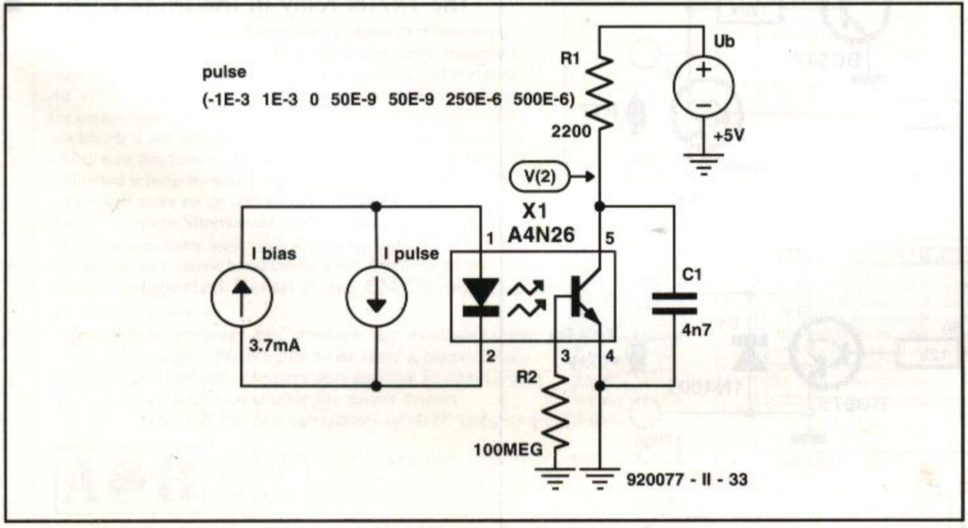


Fig. 25. Model used by Pspice for computing the characteristic in Fig. 24.

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*Electrically isolated RS232 interface. *Elektor Electronics*, March 1993.

***Further reading*:**

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Designers may also note that Rohde & Schwarz's Type ESHS 10 and ESVS 10 test receivers are now available from Livingstone Hire. These instruments meet the measurement requirements of European EMC Standards incl. 55 011 to 55 022, ETS, FCC, VCCI and VDE 0871 to 0879. Full information on these versatile instruments from Livingstone Hire, Livingstone House, Queens Road, Teddington TW11 0LB, England. Telephone (0)81 943 5151; Fax (0)81 977 6431.

CW COMPATIBLE T/R SWITCH

The use of CW (morse) on a high-power transmitter/receiver presents a serious risk of burned antenna (coax) relay contacts or destruction of a GaAs FET preamplifier. Fortunately, that problem can be overcome quite easily at a very small outlay with the circuit described here.

Design by Pedro Wyns, ON4AWQ

ALTHOUGH a number amateur radio magazines have recently carried designs that ensure that antenna relays change before the transmitter is powered, most of these circuits are suitable for 'phone' (voice) transceivers only. Just in case you did not know, early switching of the antenna relay is necessary to protect the expensive and highly sensitive GaAs FET preamplifier(s) against the huge power produced by the transmitter.

The trouble starts if you want to use a commercial VHF or UHF transceiver for high-power, high-speed CW modes such as Meteor-scatter, Tropo-DX or EME (earth-moon-earth). These modes require high transmitter power levels and extremely sensitive preamplifiers. Unfortunately, most commercial transceivers have a built-in COR (carrier operated relay), which powers the transmitter the instant the morse key is pressed, not allowing sufficient time for the antenna relay to switch over.

The circuit shown here is connected between the microphone, CW key and the transceiver. The operation of the circuit is quite simple: in 'phone' mode, the antenna relay is energized the instant the PTT switch on the microphone is pressed. The transmitter, however, is switched on a little later by a timer built around Schmitt-trigger NAND gate IC1c. When the PTT switch is released, the reverse takes place: the transmitter is switched off immediately, while the relay is de-energized a little later because of the delaying action of gate IC1d.

When CW is used, the key signals are blocked by wired-AND gate IC1a-T2 until the delay introduced by timer IC1c has elapsed (approx. 200 ms). The circuit around IC1b provides a 'hang' time of about 2 seconds to prevent relay clatter while the transmitter is being keyed. Transistors T4 is a darlington type to enable relays 'outside' the transceiver to be controlled also. If this is not required, the BD675 may be replaced by a BC547. Note that the collector of T5 is supplied via the coil of the Tx/Rx relay in the transceiver. ■

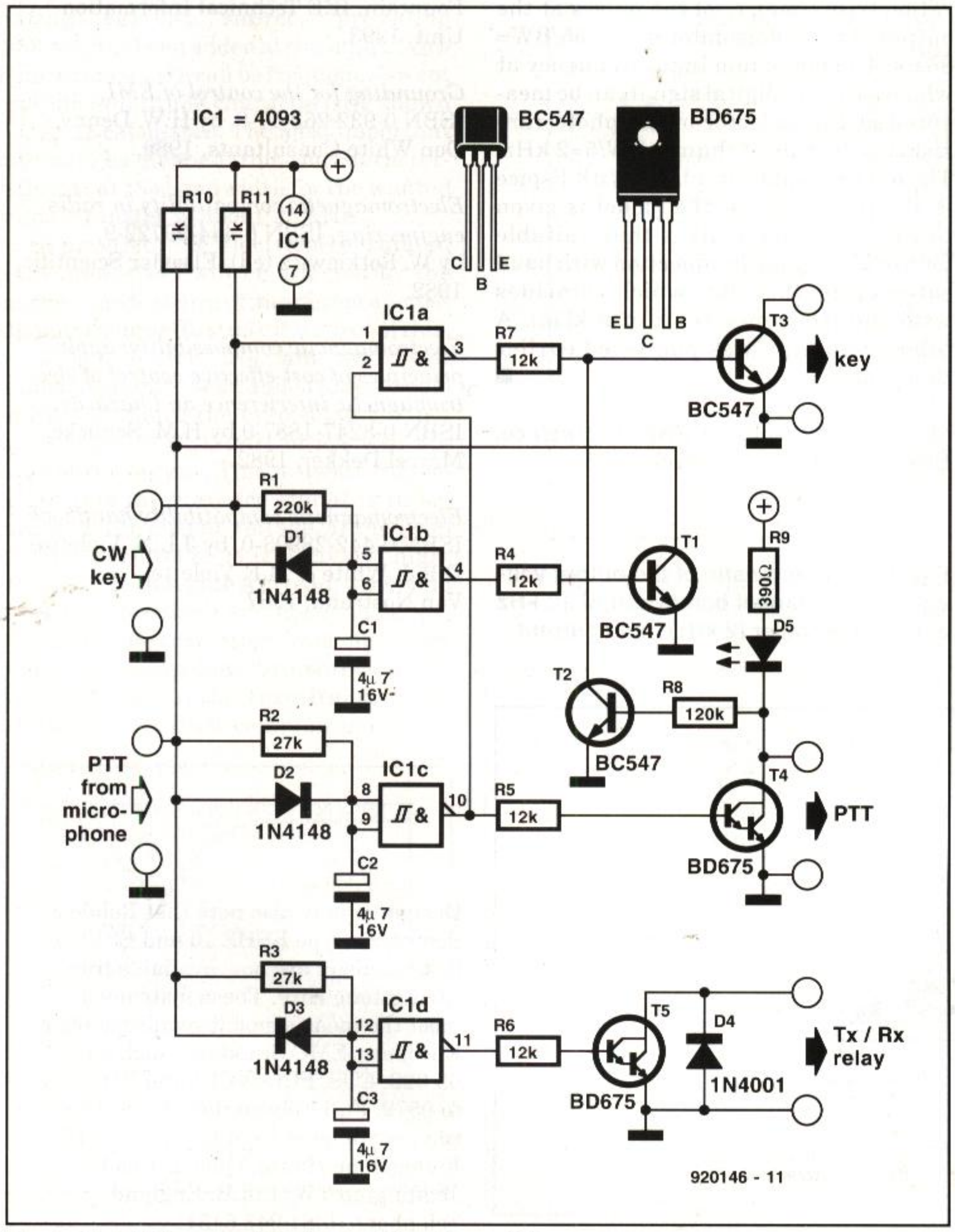


Fig. 1. Circuit diagram of the transmit/receive switch

80C32 COMPUTER APPLICATION NOTES - 3

Following the eight-instalment '8051/8032 assembler course' featured in last year's issues of *Elektor Electronics*, this column presents design ideas, programming examples and hardware experiments based on and around the popular 80C32 single-board computer. All descriptions are kept as brief as possible to ensure that a wide variety of subjects can be presented. Apart from the knowlegde you have hopefully gathered from the assembly language course, you will need the following to get going with the application notes: an 80C32 SBC (with extension board) running the EMON51 system monitor from EPROM, and a PC running the EASM51 assembler. Both programs are contained on the assembler course diskette, no. 1661. This month Zoran Stojsavljevic tells us all about 8751-to-EEPROM interfacing.

X2404 EEPROM interfacing to an 8751

Design by Zoran Stojsavljevic

XICOR's X2404 is a 4096-bit serial electrically erasable PROM (EEPROM), internally organized as two pages, each containing 256×8 bits. The X2404 features a serial interface and an I2C compatible software protocol that allows it to be operated via a 2-wire bus. The pinning and internal architecture of the IC are given in Fig. 1. The SCL (serial clock) input is used to clock all data into and out of the device. The serial data pin, SDA, is bidirectional, and used to transfer data into and out of the device. SDA is an open-drain output, and may be wire-ORed with any number of open-drain or open-collector outputs to form a bus. Address input A0 is not used by the X2404, although it must be tied to V_{ss} for proper device operation. Address inputs A1 and A2 are used to set the least-significant two bits of the six-bit slave address assigned to the device. The address inputs are static, and should be tied to logic high or low levels, to give one unique address per device.

The circuit diagram in Fig. 2 shows an example application of the X2404 in a 8751 microcontroller driven racing car computer. The functions of this computer are not our prime concern here, hence the following discussion will concentrate mainly on the way the 8751 and the X2404 are set up to communicate properly. The functions of the four push-buttons are:

S2: adjust clock;
S3: display max. rpm during race;
S4: display max. rpm ever.
S5: reserved.

The hardware implementation of the X2404 is simplicity itself, being essentially restricted to two lines only. In the application circuit, the X2404 records the highest rpm (revolutions per minute) value of the car engine. This is achieved by reducing the ignition pulses to a suitable level, digitizing (Tx), and feeding them to the P3.2 input of the 8751 microcontroller.

X2404 device operation

The X2404 supports a bidirectional, bus oriented protocol. This protocol defines any device that sends data on to the bus as a transmitter, and the receiving device as a receiver. The device controlling the data transfer is a master, and the device being controlled is a slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X2404 will be considered a slave in all applications.

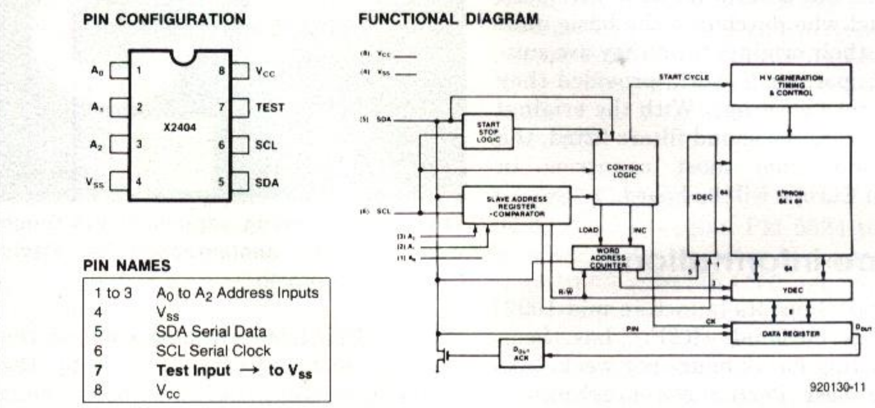


Fig. 1. Pin layout and internal structure of EEPROM X2404.

Data states on the SDA line can change only when SCL is low. SDA changes during SCL 'high' periods are reserved for indications of start and stop conditions, as illustrated in Fig. 3. All commands are preceded by the start condition, which is a high-to-low transition of SDA when SCL is high. The X2404 continuously monitors the SDA and SCL lines for the start condition, and will not respond to any command until this condition is satisfied. All communications are terminated by a stop condition, which is a low-to-high transition of SDA when SCL is high. The definitions of the start and stop conditions are illustrated in Fig. 4.

The transmitting device, either a master or a slave, releases the bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line low to acknowledge that it received the eight bits of data. The X2404 will always respond with an acknowledge after recognition of a start condition, followed by its slave address. If both the device and a write operation have been selected, the X2404 will respond with an acknowledge on receipt of each subsequent

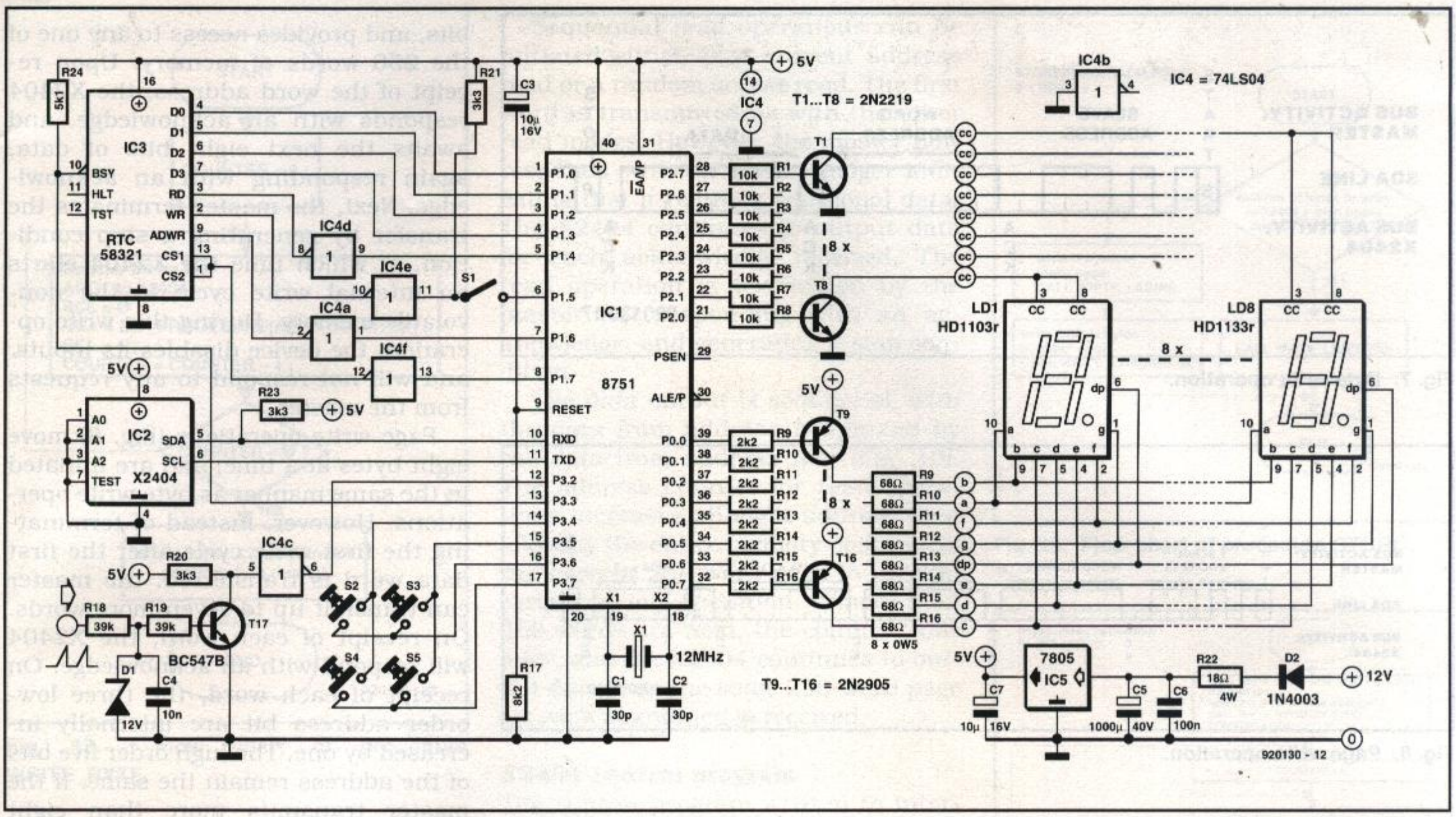


Fig. 2. Application of an X2404 in a car computer based on Intel's 8751 microcontroller. The X2404 serves, among others, to store and retain the highest rpm of the car's engine.

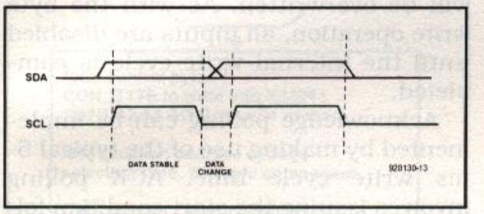


Fig. 3. Clock and data conventions.

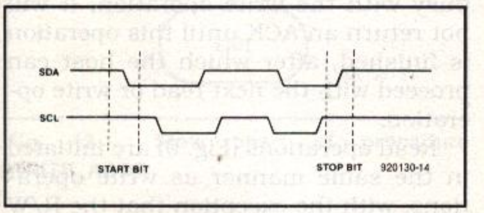


Fig. 4. Definition of start and stop conditions.

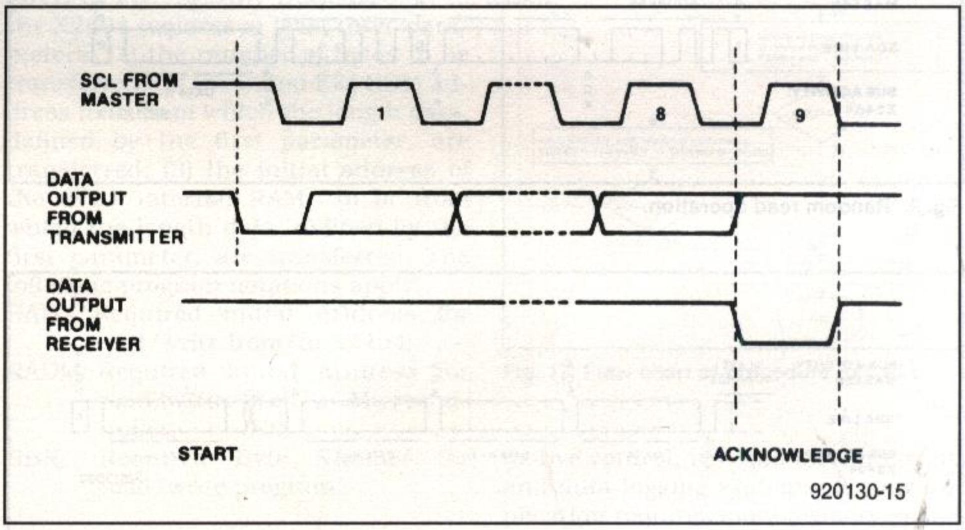


Fig. 5. Response from the receiver.

eight-bit word (Fig. 5). In read mode, the X2404 will transmit eight data bits, release the SDA line, and monitor it for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X2404 will continue to transmit data. If an acknowledge is not detected, the X2404 will terminate further data transmissions, and await the stop condition.

Following a start condition, the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the type identifier (see Fig. 6). For the X2404 this is fixed as 1010. The next two bits, A2 and A1, address one of up to four X2404s connected on to the bus. The next bit, A0, allows the host to toggle between the two 256-word pages contained in the X2404. The last bit in the device address field switches between read (bit=1) and write (bit=0) operations. Following the start condition, the X2404 monitors the SDA bus, comparing the slave address being transmitted with its own address (i.e., four-bit device type and two-bit device number). When the two match, the X2404 generates an acknowledge on the SDA line. Depending on the state of the R/W bit, the device next does a read or a write operation.

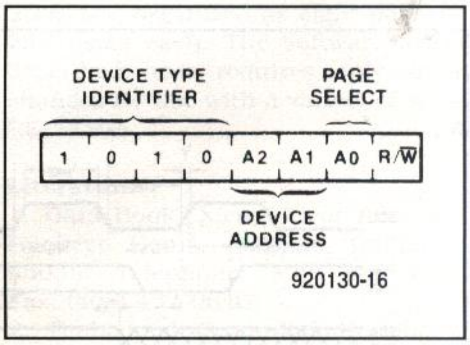


Fig. 6. Address format.

Write operations on the X2404 can be divided into two types: byte write and page write. For a byte write operation (Fig. 7), the X2404 requires a second address field, which forms the word address. This consists of eight

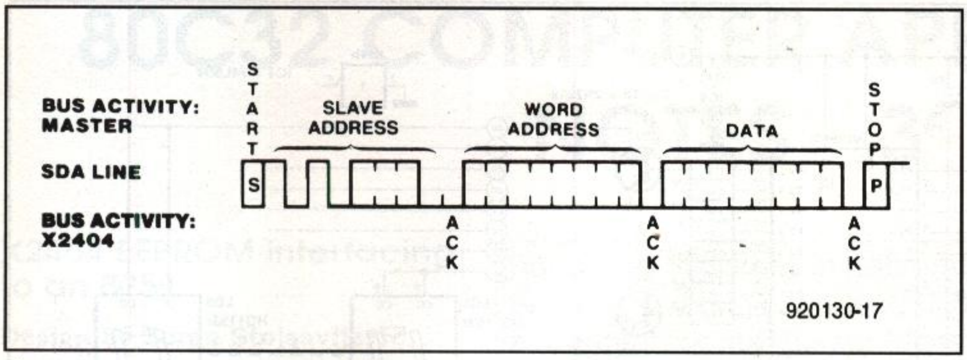


Fig. 7. Byte write operation.

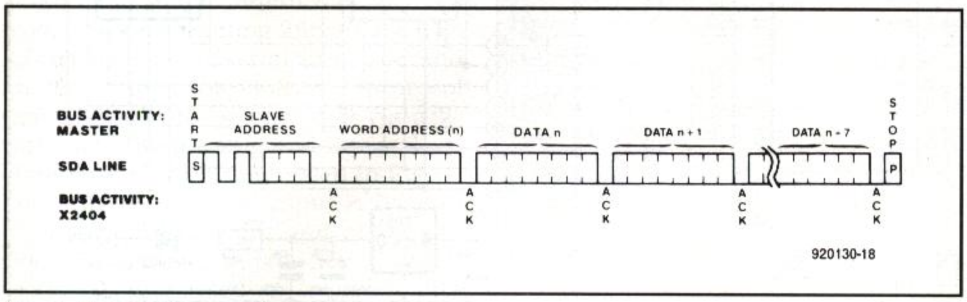


Fig. 8. Page write operation.

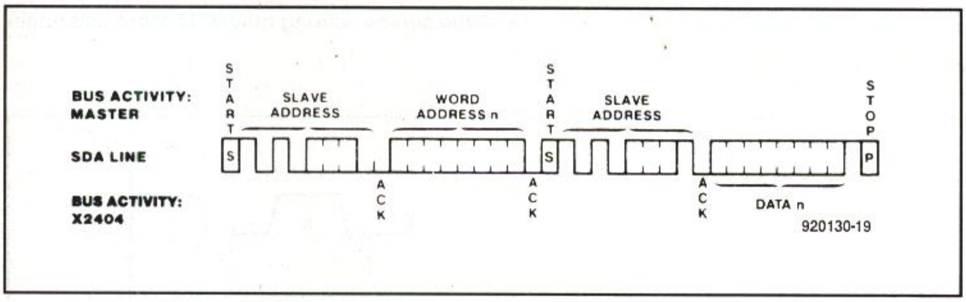


Fig. 9. Random read operation.

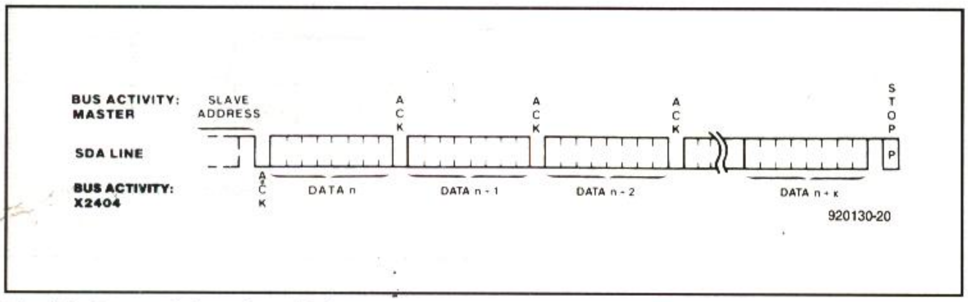


Fig. 10. Sequential read operation.

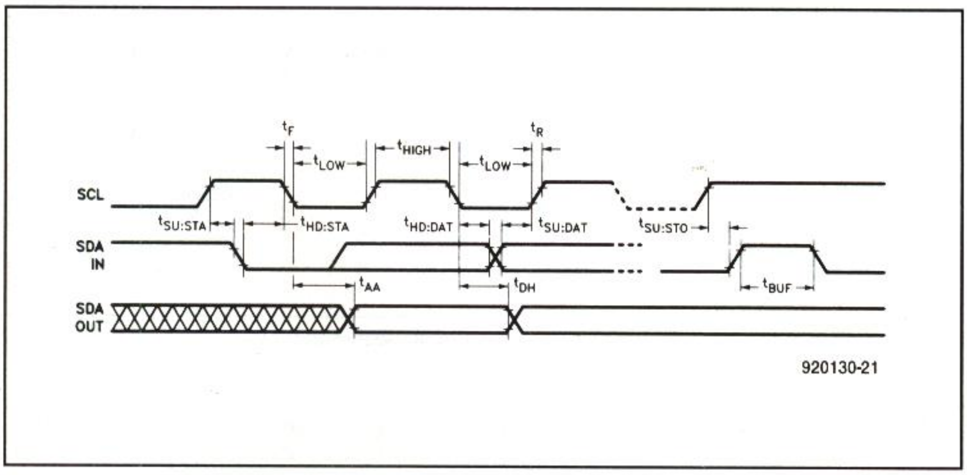


Fig. 11. Control and data line setup times.

bits, and provides access to any one of the 256 words of memory. Upon receipt of the word address, the X2404 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. Next, the master terminates the transfer by generating a stop condition, at which time the X2404 starts an internal write cycle to the non-volatile memory. During this write operation, the device disables its inputs, and will not respond to any requests from the master.

Page write operations (Fig. 8) move eight bytes at a time, and are initiated in the same manner as byte write operations. However, instead of terminating the first write cycle after the first data word is transferred, the master can transmit up to seven more words. On receipt of each word, the X2404 will respond with an acknowledge. On receipt of each word, the three low-order address bit are internally increased by one. The high order five bits of the address remain the same. If the master transmits more than eight words before generating the stop condition, the address counter will 'roll over', and the previously stored data will be overwritten. As with the byte write operation, all inputs are disabled until the internal write cycle is completed.

Acknowledge polling can be implemented by making use of the typical 5-ms write cycle time. ACK polling involves issuing the start condition followed by the slave address for a write operation. If the relevant X2404 is still busy with the write operation, it will not return an ACK until this operation is finished, after which the host can proceed with the next read or write operation.

Read operations (Fig. 9) are initiated in the same manner as write operations, with the exception that the R/W bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/W bit set to one, the master must perform a 'dummy' write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately re-issues the start condition and the slave address with the R/W bit set to one. This will be followed by an acknowledge from the X2404, and then by the 8-bit word. The master does not acknowledge the transfer, but generates a stop condition, so that the X2404 stops transmitting.

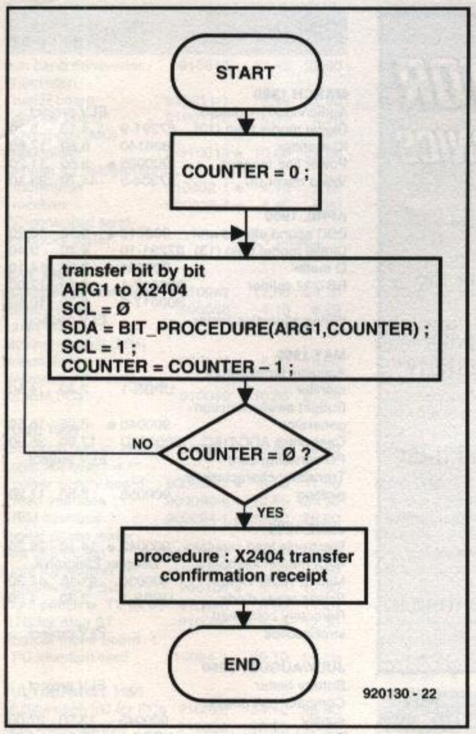


Fig. 12. Flow chart of procedure WRITE_BYTE.

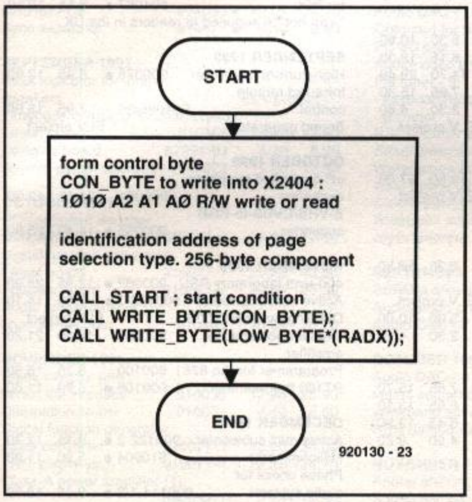

START
form control byte
CON_BYTE to write into X2404 :
1010 A2 A1 A0 R/W write or read
identification address of page
selection type. 256-byte component
CALL START ; start condition
CALL WRITE_BYTE(CON_BYTE);
CALL WRITE_BYTE(LOW_BYTE*(RADX));
END
920130 - 23

Fig. 13. Flow chart of procedure WRITE_ADDR.

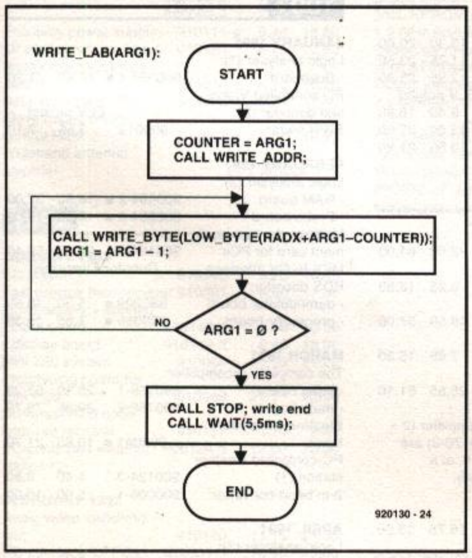


Fig. 14. Flow chart of procedure WRITE_LAB.

Sequential read operations can be initiated either as a current address read or a random access read. The first word is transmitted as with the other read modes. However, the master now responds with an acknowledge, indicating that it requires additional data. The X2404 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge, and generating a stop condition.

The data output is sequential, with the data from address *N* followed by the data from address *N+1* (Fig. 10). The address counter for read operations increases all eight address bits, allowing the entire memory contents of the current 256-word page to be read serially in one operation. If more than 256 words are read, the counter 'rolls over', and the X2404 continues to output data from the same 256-word page for each acknowledge received.

X2404 control program

The control program written to interface the X2404 to an 8751 is based on the previously discussed device operation and the timing specifications given in Fig. 11. Any transmission to the X2404 requires at least three parameters: (1) the number of bytes to be transferred; (2) the initial EEPROM address to or from which the length data, defined by the first parameter, are transferred; (3) the initial address of the 8751 internal RAM to or from which the length data, defined by the first parameter, are transferred. The following program notations apply:

RADX: Required initial ADdress for read/write from/to X2404;
RADM: Required initial ADdress for read/write from/to Microcontroller;
RBN: Required Byte Number for read/write program.

The flow charts in Figs. 12 through 16 illustrate the basic operation of the X2404 control program. The flow charts were used as a starting point for the assembler code written to implement the X2404-to-8751 link. Unfortunately, owing to lack of space, it is not possible to print the assembly listing of the interface program. The program is available on an MS-DOS formatted disk, however, and be obtained through the Readers Services — the order code is **1891**.

Conclusion

The X2404 EEPROM and the software driver developed for it allows an 8051 (or derivate) microcontroller to store a relatively small packet of data that is not lost when the power is switched off. Applications june be found in automotive control, test and measurement, and data logging systems. If your application requires more memory space, there are EEPROMs in the X24xx family with a larger capacity, for instance, the X24C16 with a capacity of 2 kBytes, organized as eight pages of 256 bytes each. The software driver described here requires only small changes for use with a variety of serial EEPROMs. ■

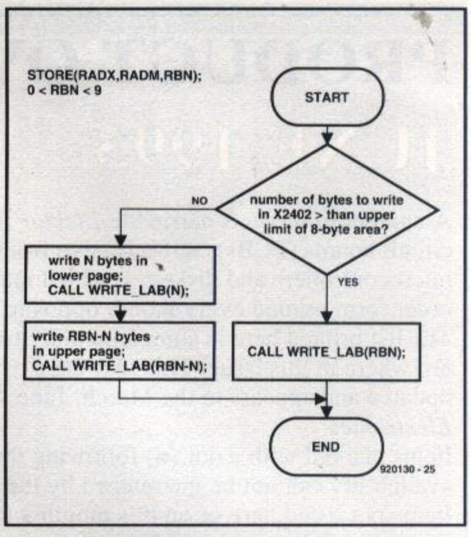

STORE(RADX,RADM,RBN);
0 < RBN < 9
START
NO
number of bytes to write in X2402 > than upper limit of 8-byte area?
YES
write N bytes in lower page;
CALL WRITE_LAB(N);
write RBN-N bytes in upper page;
CALL WRITE_LAB(RBN-N);
CALL WRITE_LAB(RBN);
END
920130 - 25

Fig. 15. Flow chart of procedure STORE.

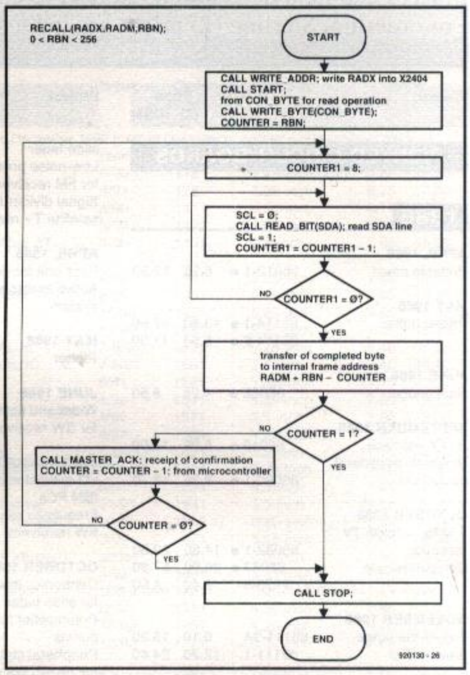

RECALL(RADX,RADM,RBN);
0 < RBN < 256
START
CALL WRITE_ADDR; write RADX into X2404
CALL START;
from CON_BYTE for read operation
CALL WRITE_BYTE(CON_BYTE);
COUNTER = RBN;
COUNTER1 = 8;
SCL = 0;
CALL READ_BIT(SDA); read SDA line
SCL = 1;
COUNTER1 = COUNTER1 – 1;
NO
COUNTER1 = 0?
YES
transfer of completed byte to internal frame address
RADM + RBN – COUNTER
NO
COUNTER = 1?
YES
CALL MASTER_ACK; receipt of confirmation
COUNTER = COUNTER – 1; from microcontroller
NO
COUNTER = 0?
YES
CALL STOP;
END
920130 - 26

Fig. 17. Flow chart of procedure RECALL.

Literature:

1. Data Book, Xicor. Xicor Inc., 851 Buckeye Court, Milpitas, California 95035. Telephone (408) 432-8888. Fax: (408) 432-0640.
2. Embedded Controller Handbook, Intel Corp.

Note:

Figures 1, and 3 through 11, and extracts from X2404 datasheets reproduced by courtesy of Xicor, Inc.

Construction

The VU meter is most conveniently built on the printed-circuit board shown in Fig. 5. Start with cutting off the display section if that is to be located elsewhere. Then, all components can be fitted. Note that most resistors and all diodes should be mounted upright. The 270 pF, 470 pF and 680 pF capacitors must be polystyrene types to prevent too high damping of the filters. These capacitors must also be mounted upright.

Once the boards have been completed, they must be interlinked by an angled header (see photograph on p. 8) or 17 discrete, short wires.

The power for the meter may be drawn from the equipment into which it is built, but, owing to the current requirement on the positive line, it is best to build a small, separate supply.

If a larger display is used than shown on the PCB, it must be connected to the board via suitable connectors or half IC sockets. The display section of the board is then useless.

When a small display is used, jumper JP_1 on the board must be placed in position 'H'. Resistors R_{41} and R_{43} must be replaced by a wire bridge.

PARTS LIST

Resistors:
R1=1 kΩ
R2=2.2 kΩ
R3=10 kΩ
R4, R5, R6, R14, R19, R24=301 kΩ, 1%
R7, R12, R17, R22, R27, R32, R37=51.1 kΩ, 1%
R8, R13, R18, R23, R28, R33, R38=4.7 MΩ
R9=309 kΩ, 1%
R10, R34=18.2 kΩ, 1%
R11=619 kΩ, 1%
R15, R20, R25=17.8 kΩ, 1%
R16, R21, R26=604 kΩ, 1%
R29=294 kΩ, 1%
R30=17.4 kΩ, 1%
R31=590 kΩ, 1%
R35=6.49 kΩ, 1%
R36=118 kΩ. 1%
R44, R45=390 Ω
R46=1.0 kΩ, 1%
R47=30.9 kΩ, 1%
R48–R57=330 Ω
R58=1 MΩ
R59=68 kΩ
R60=2.2 Ω
P1=47 kΩ preset
P2=2.5 kΩ preset

Capacitors:
C1, C5, C6=12 nF
C2=33 nF
C3, C11, C12=1.8 nF
C4, C7, C10, C13, C16, C19, C24=100 nF
C8, C9=4.7 nF
C14, C15=680 pF*
C17, C18=270 pF*
C20, C21, C22=470 pF*
C29=100 pF
C30=1 nF
C31–C40, C44=47 nF, ceramic
C41, C42, C43, C45, C46=100 nF, ceramic
*polystyrene, axial

Semiconductors:
D1, D2, D4, D7, D10, D13, D16, D19, D22=1N4148
D3, D5, D6, D8, D9, D11, D12, D14, D15, D17, D18, D20, D21, D23=BAT85
IC1=TL081
IC2–IC5=TL084
IC6, IC7=4051
IC8=4060
IC9=TLC272
IC10=UDN2585A
IC11, IC12=LM3915

Miscellaneous:
JP1=terminal strip with 3-way jump lead
K1=audio socket
LD1, LD2=display with 5×7 matrix, e.g., Kingbright Type TC07-11EWA (larger types: TC20-11EWA; 5×8:TC24-11EWA
PCB Type 920151 (see p. 70)

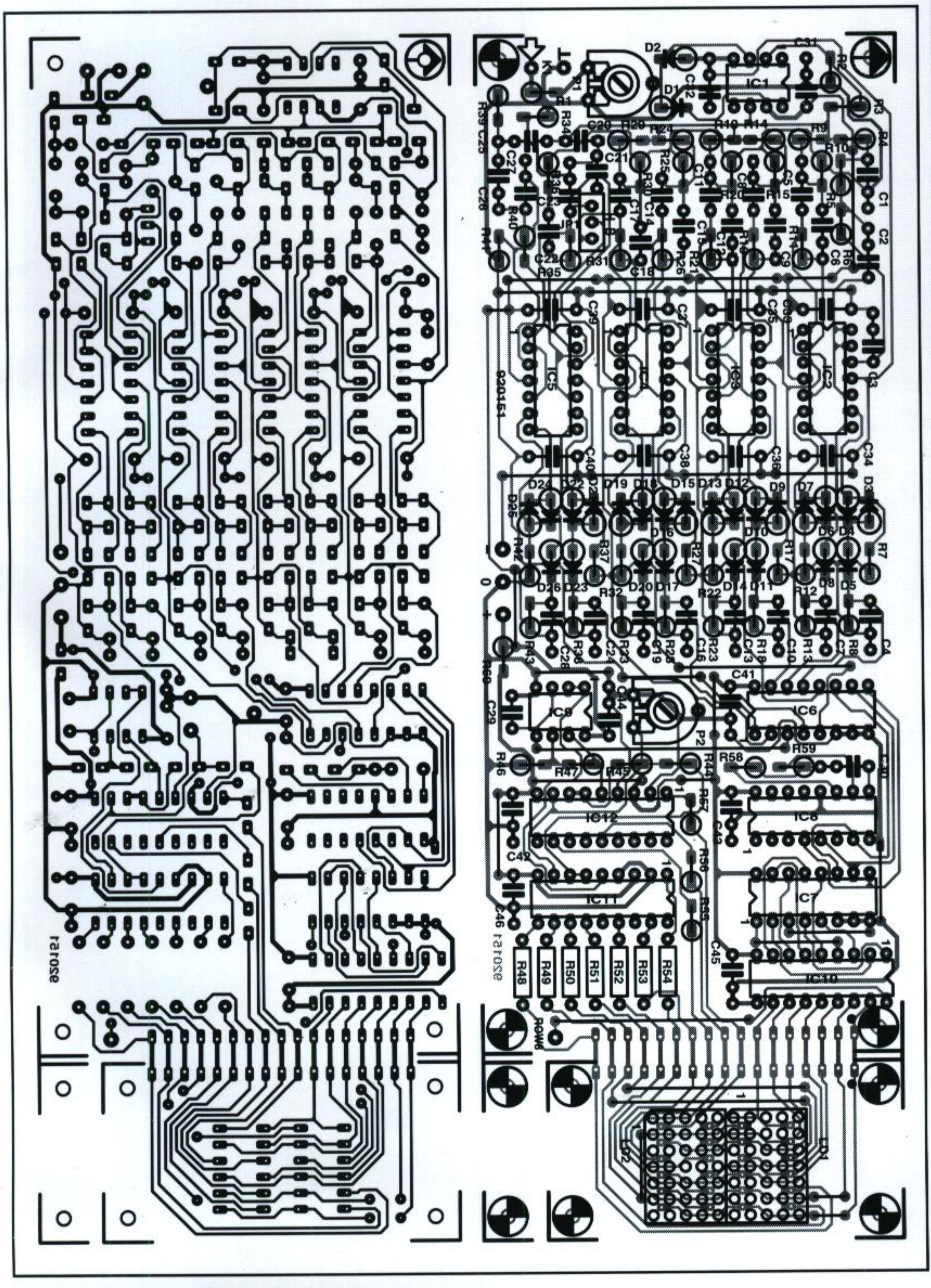


Fig. 4. The printed-circuit board for the VU meter.

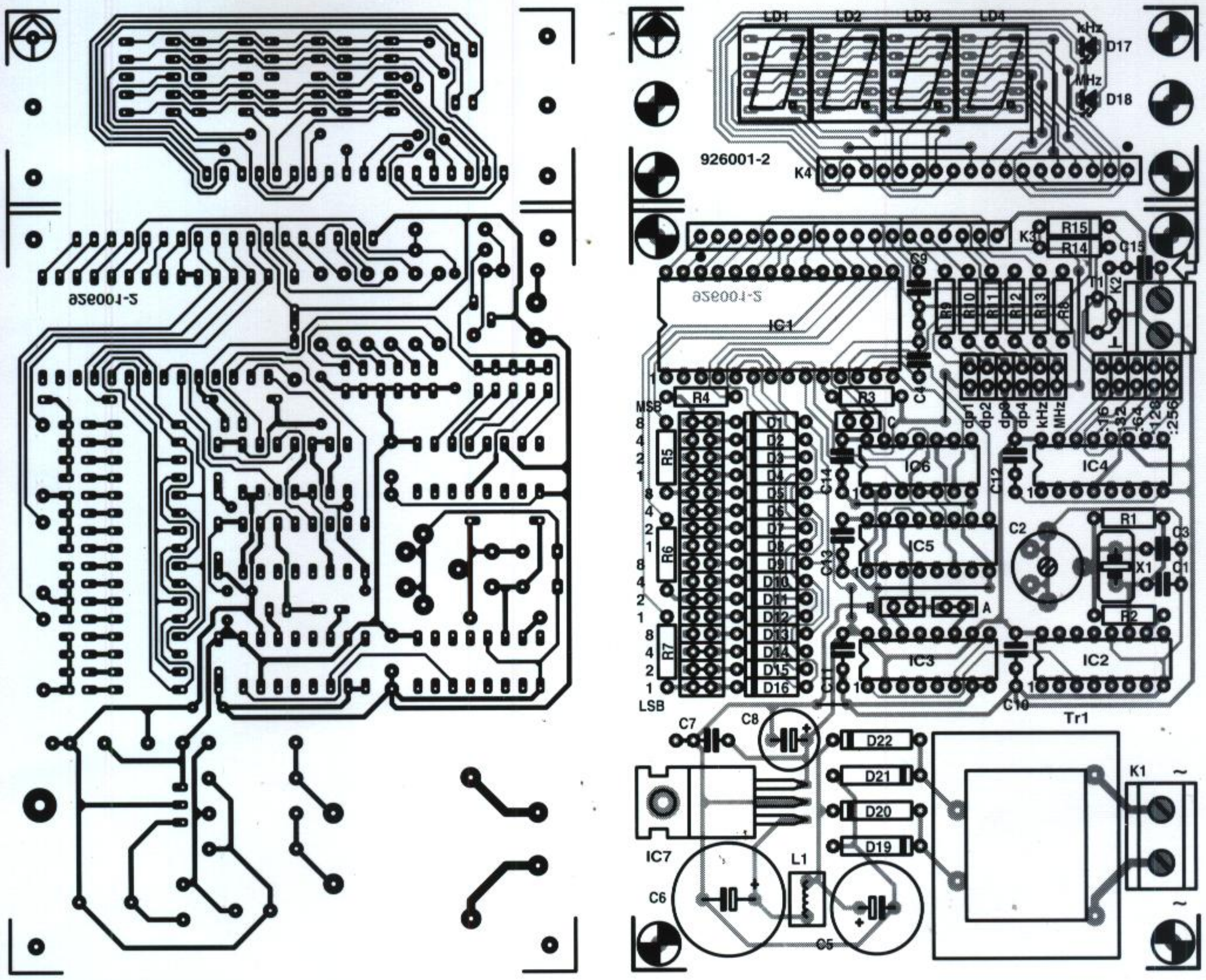
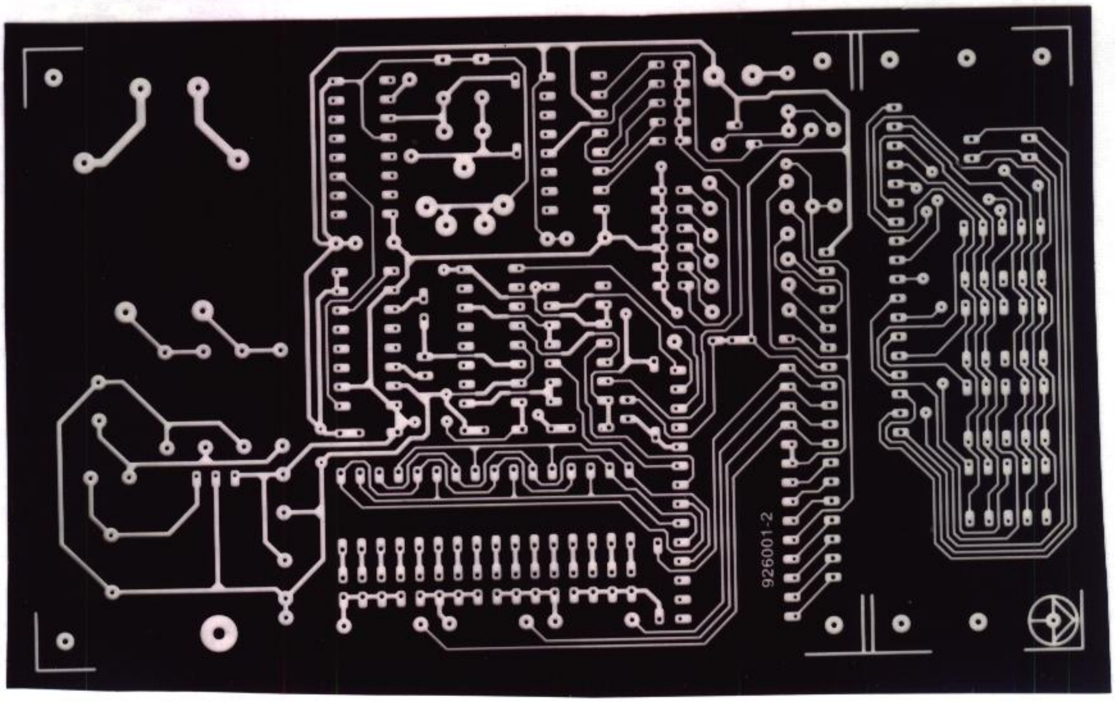


Fig. 4. Track layout (mirror image) and component mounting plan of the printed circuit board designed for the frequency meter.



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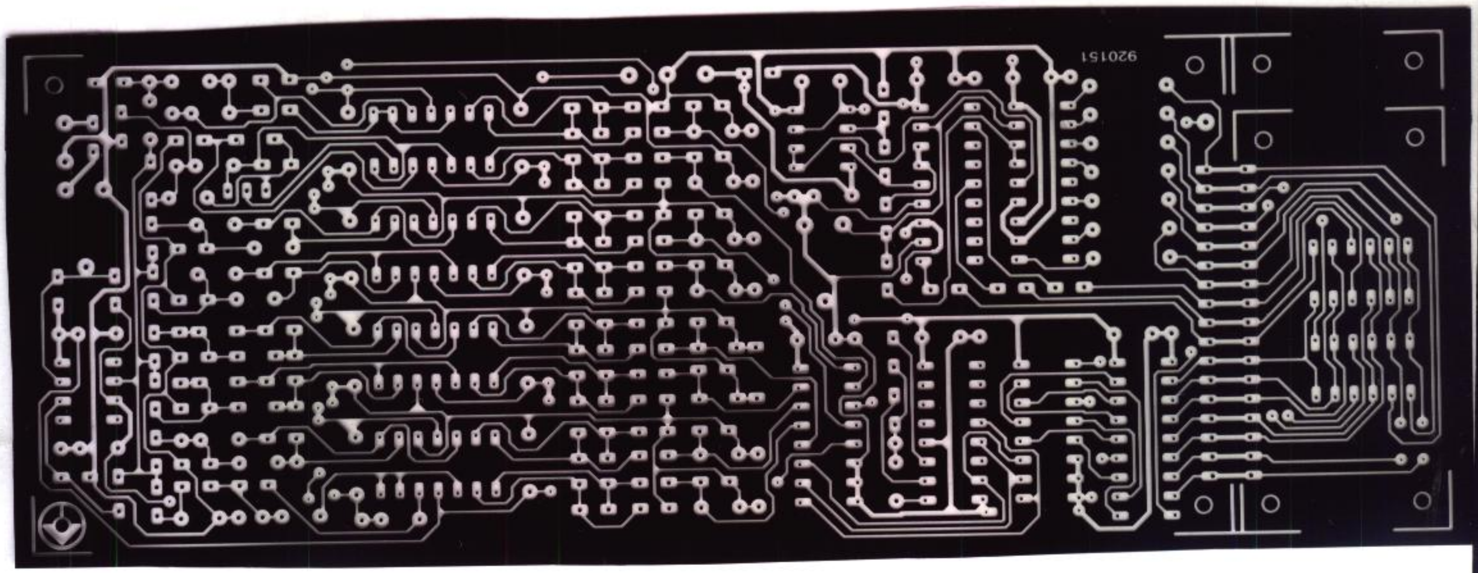

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